Interconnect exploration for future wire dominated technologies

Case study:

A.Papanikolaou, M. Miranda, F. Catthoor, H. Corporaal, H.De Man
D.De Roest, M. Stucchi, K. Maex

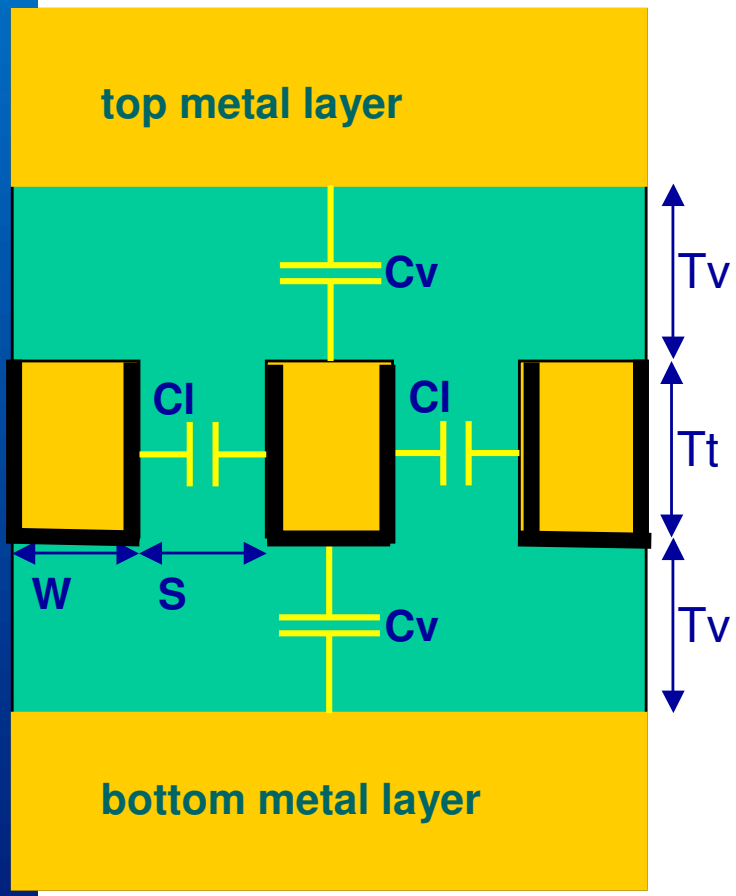
IMEC/K.U.Leuven

Karen.Maex@imec.be

Outline

- State of the art and issues in Cu low k
- Consequences for wiring hierarchy
- Extended wiring hierarchy
- Case study: SRAM memory design
- Conclusion an questions

Why Cu-low k



cross-section of inter-connect system

- **resistance**

$$R = \rho \frac{L}{W \cdot T_t} = \rho_{eff} \frac{L}{W T_t}$$

- interline capacitance

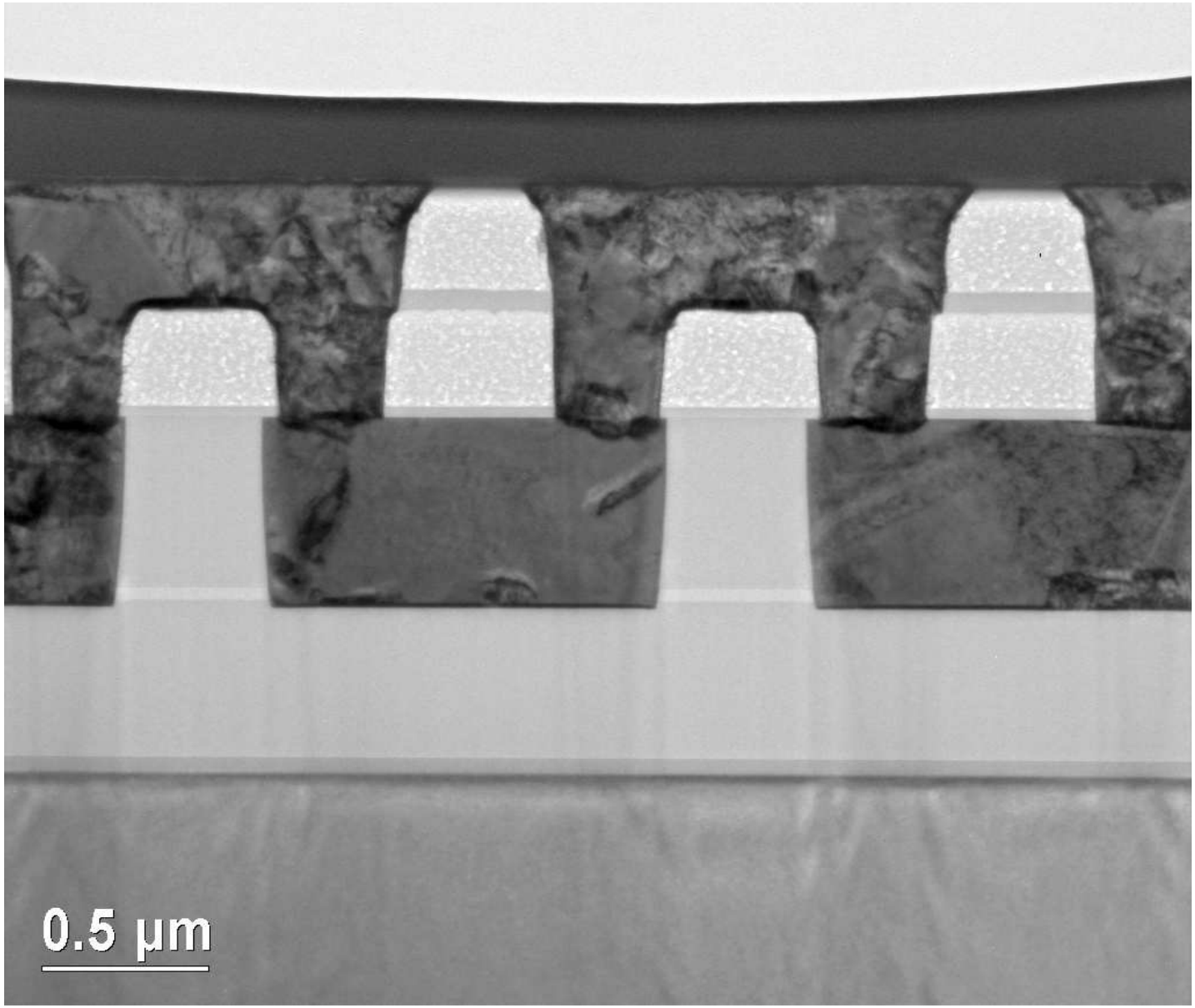
$$C_i = k_{eff-t} \varepsilon_0 \frac{L T_t}{S}$$

- interlevel capacitance

$$C_v = k_{eff-v} \varepsilon_0 \frac{L W}{T_v}$$

ρ = metal resistivity
k = relative dielectric constant
ε_0 = permittivity of free space
L = line length
T = metal / dielectric thickness

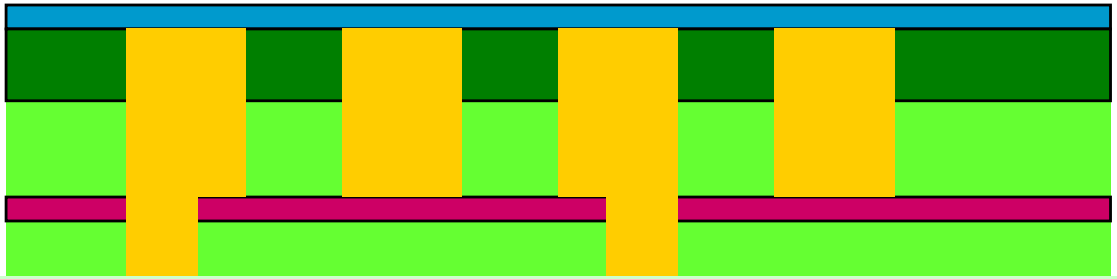
TEM X Section



ITRS roadmap: 2001 update

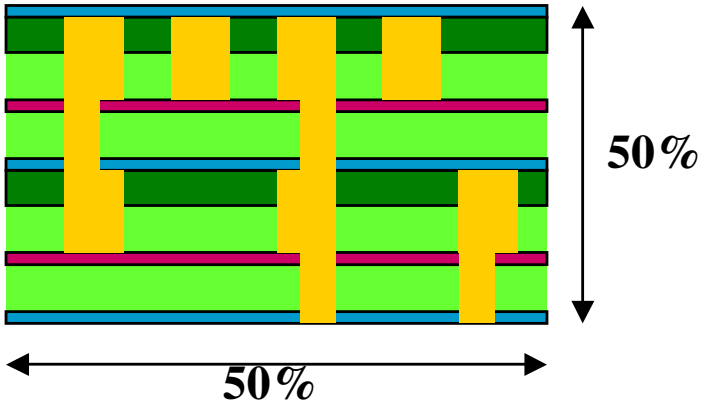
	2001	2002	2003	2004	2005	2007	2010	2013
	130nm			90nm		65nm	45nm	32nm
local wire pitch [nm]	350	295	245	210	185	150	105	75
local wire AR	1.6	1.6	1.6	1.7	1.7	1.7	1.9	2
intermediate wire pitch [nm]	450	380	320	265	240	195	135	95
intermediate wire AR line/via	1.6/1.4	1.6/1.4	1.7/1.5	1.7/1.5	1.7/1.5	1.8/1.6	1.8/1.6	1.9/1.7
global wire pitch [nm]	670	565	475	460	360	290	205	140
global wire AR line/via	2.0/1.8	2.0/1.8	2.1/1.9	2.1/1.9	2.2/2.0	2.2/2.0	2.3/2.1	2.4/2.2
barrier thickness [nm]	16	14	12	10	9	7	5	3.5
eff. resistivity [u Ohm cm]	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
number of levels	8	8	8	9	10	10	10	11
# of optional levels	2	2	4	4	4	4	4	4
bulk k	2.7	2.7	2.7	2.4	2.4	2.1	1.9	1.7
eff. K	3.0-3.6	3.0-3.6	3.0-3.6	2.6-3.1	2.6- 3.1	2.3-2.7	2.1	1.9

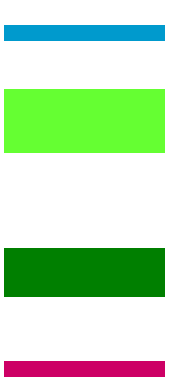
Cu-low k:state of the art
Scaling dimensions



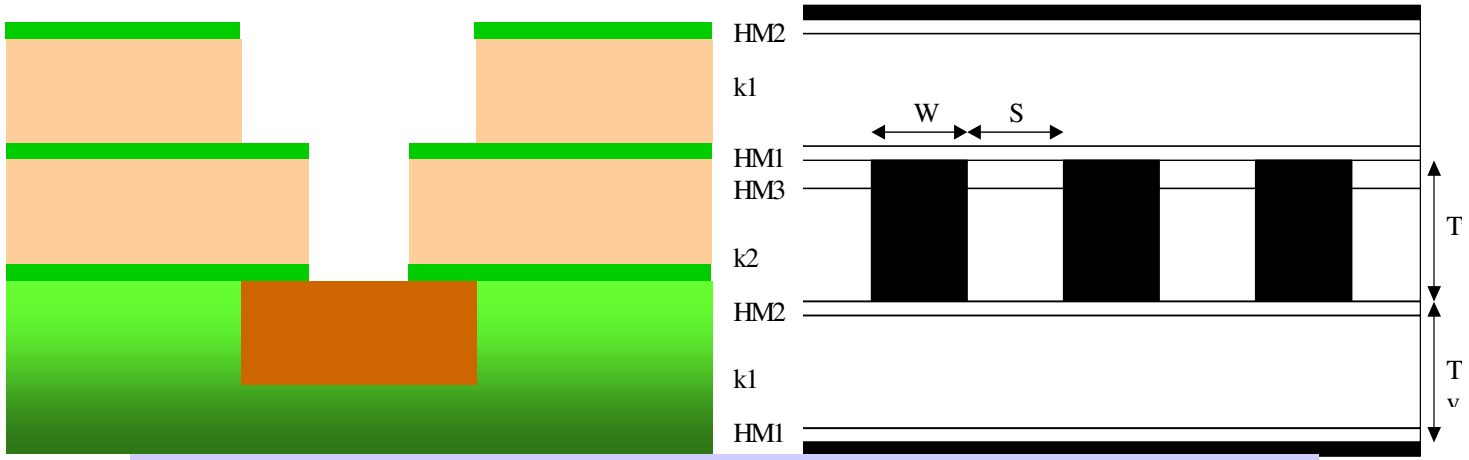
Careful definition of functionality of each layer
- tominimize its thickness
- to minimize its k-value
- without compromising its function

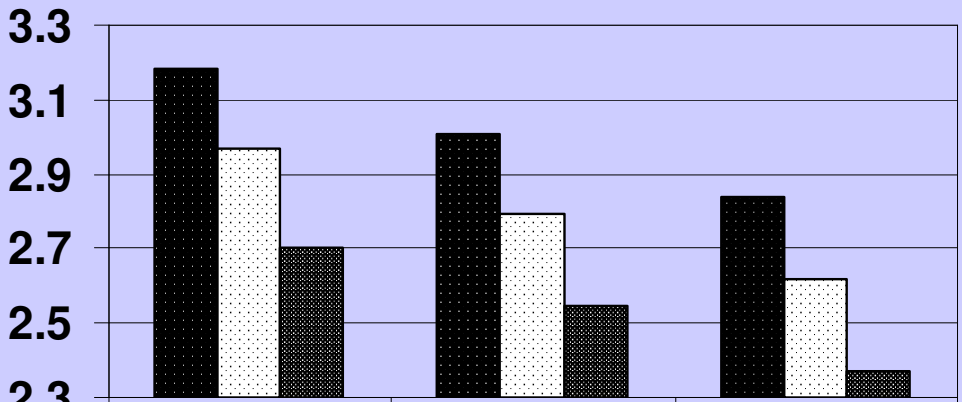
2 nodes further…





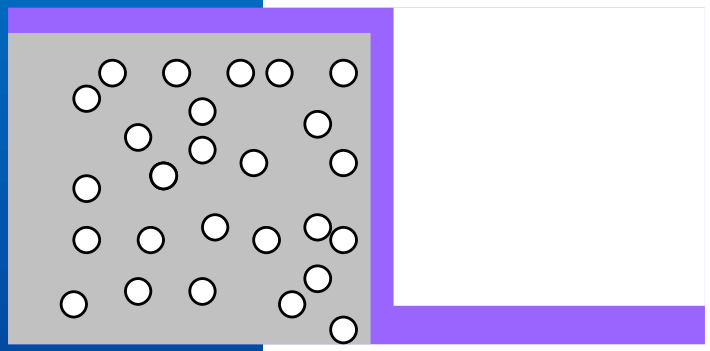
Cu-lowk: state of the art
Module integration schemes

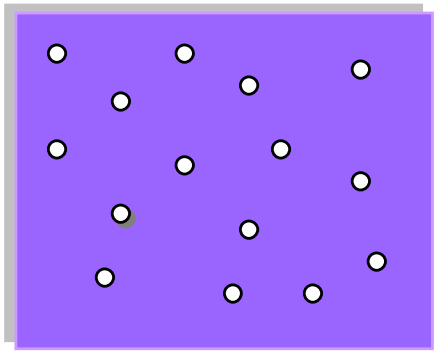


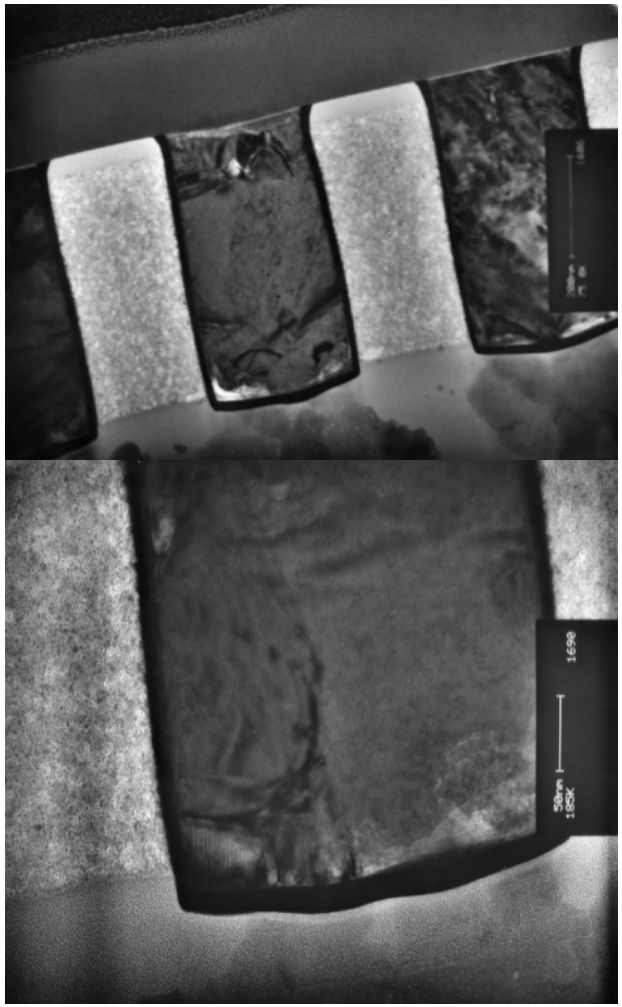


	2.7	2.4	2.1
3.3/3.3/4.5	3.18E+00	3.01E+00	2.84E+00
3.3/3.3/3.3	2.97E+00	2.79E+00	2.62E+00
2.7/2.7/2.7	2.70E+00	2.55E+00	2.37E+00

Cu/low k: state of the art





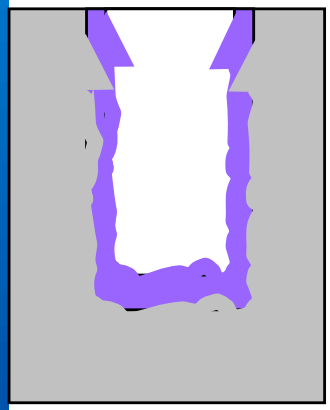


Barrier
= sealing layer for pores
= adhesion layer on low k dielectrics
= diffusion barrier
= adhesion layer for Cu

= a few atomic layers thick: atomic layer control!

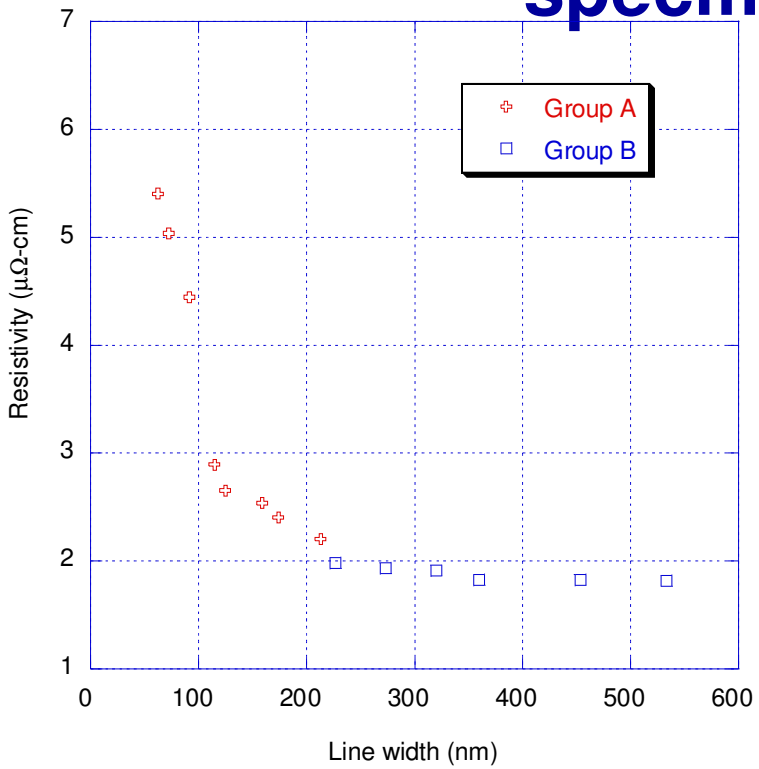
Barrier integrity

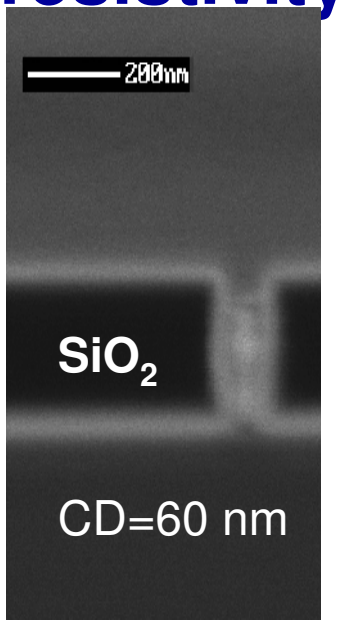
Cu-low k: state of the art: specific resistivity



Filling down to 60 nm line-width is proven

Patterning: E-beam (GroupA), DUV (GroupB)





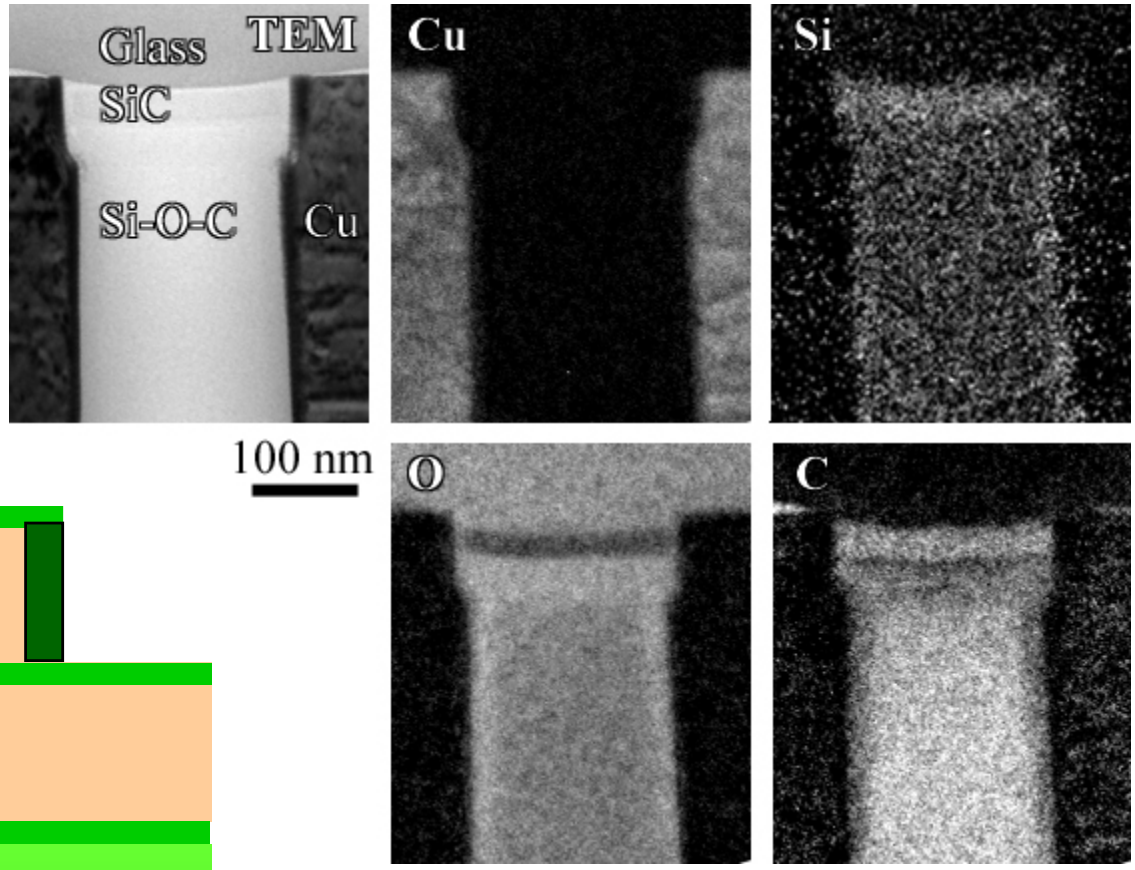
AR=6.7

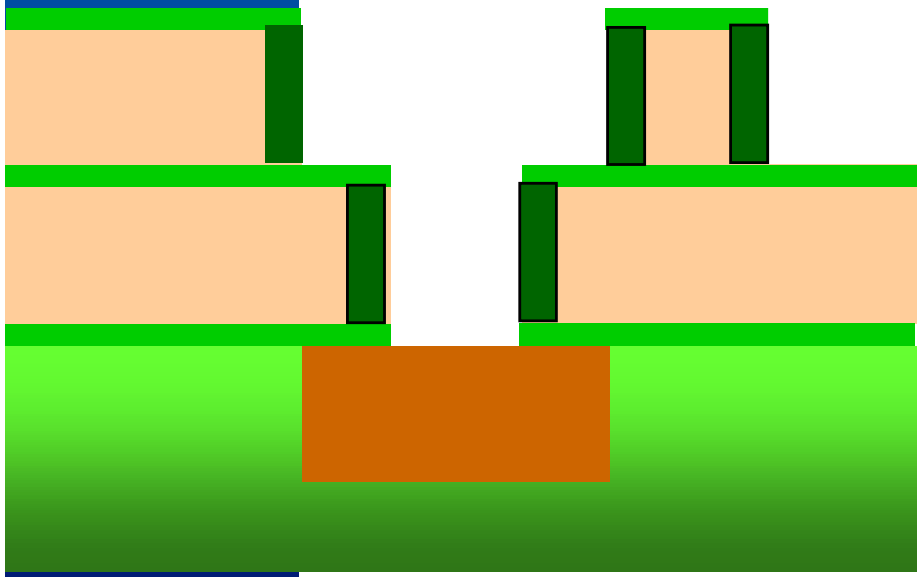
- inelastic scattering at Cu-barrier sidewall
- becomes important for dimensions on order of mean free path of electrons in Cu
-roughness on scale of wavelength of electrons in Cu

- Size effect --Fuchs' theory:scattering factor p

- Grain boundary scattering --Mayadas' theory reflection coefficient R

Cu/low k:state of the art

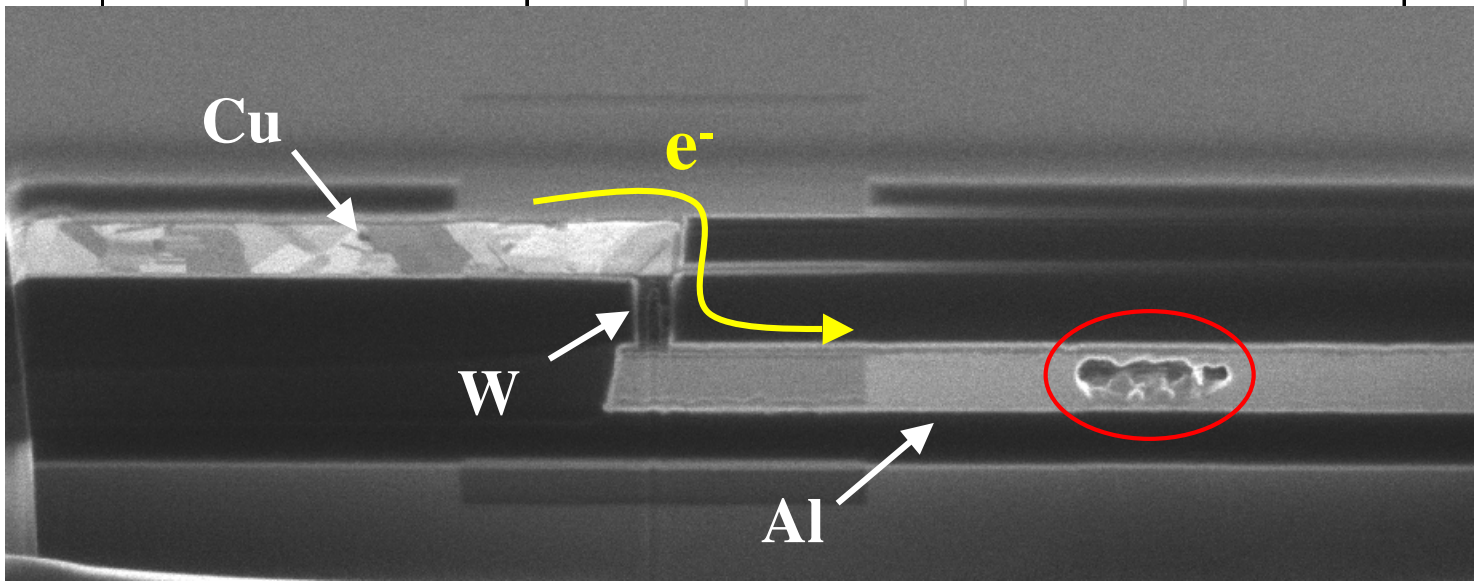




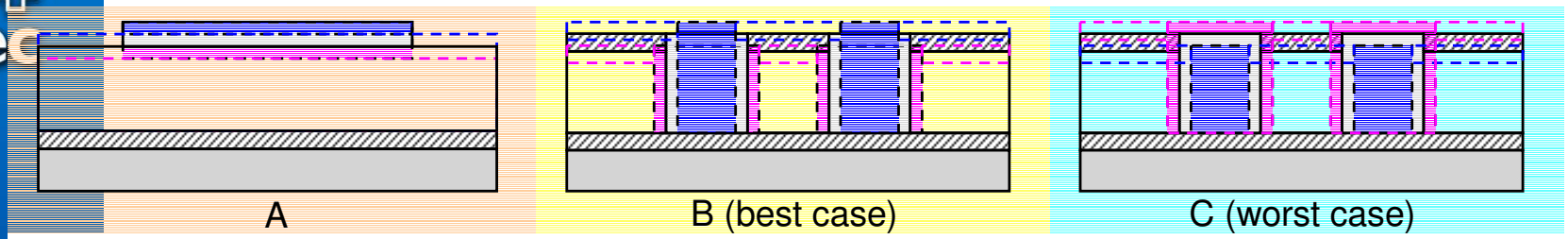
-k-value for <100nm spacing?

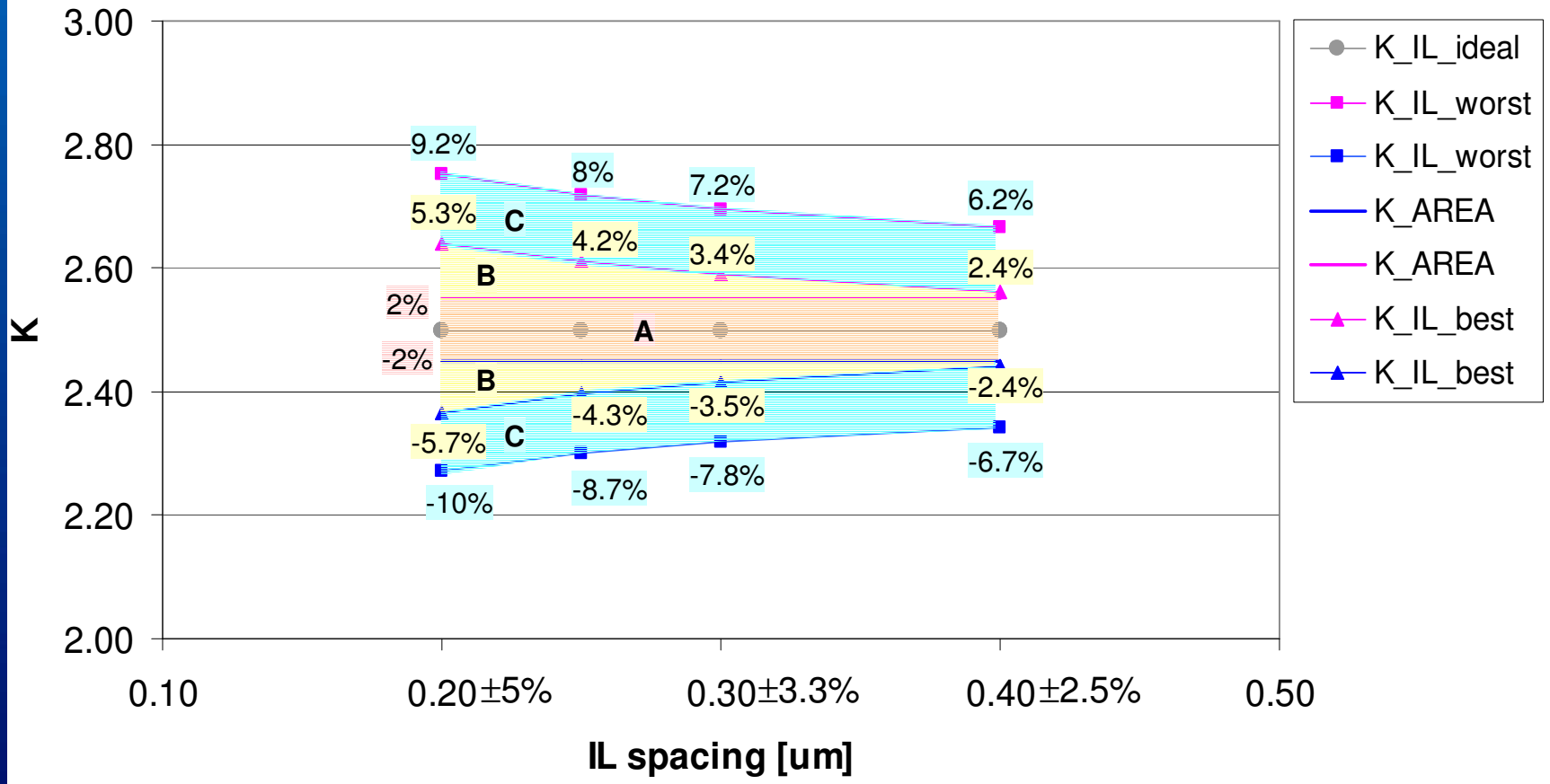
Cu-low k: state of the art Electromigration

	2004	2007	2010	2013
	90nm	65nm	45nm	32nm
ID nMOS [μA/mm]				
LOP	600	700	700	800
HP	900	900	1200	1500
Imax (via) mA	0.24	0.18	0.1	0.07
at 105C				
Jmax (wire) [A/cm2]	1.50E+06	2.10E+06	2.70E+06	3.30E+06
at 105C				



Cu-low k: state of the art process control





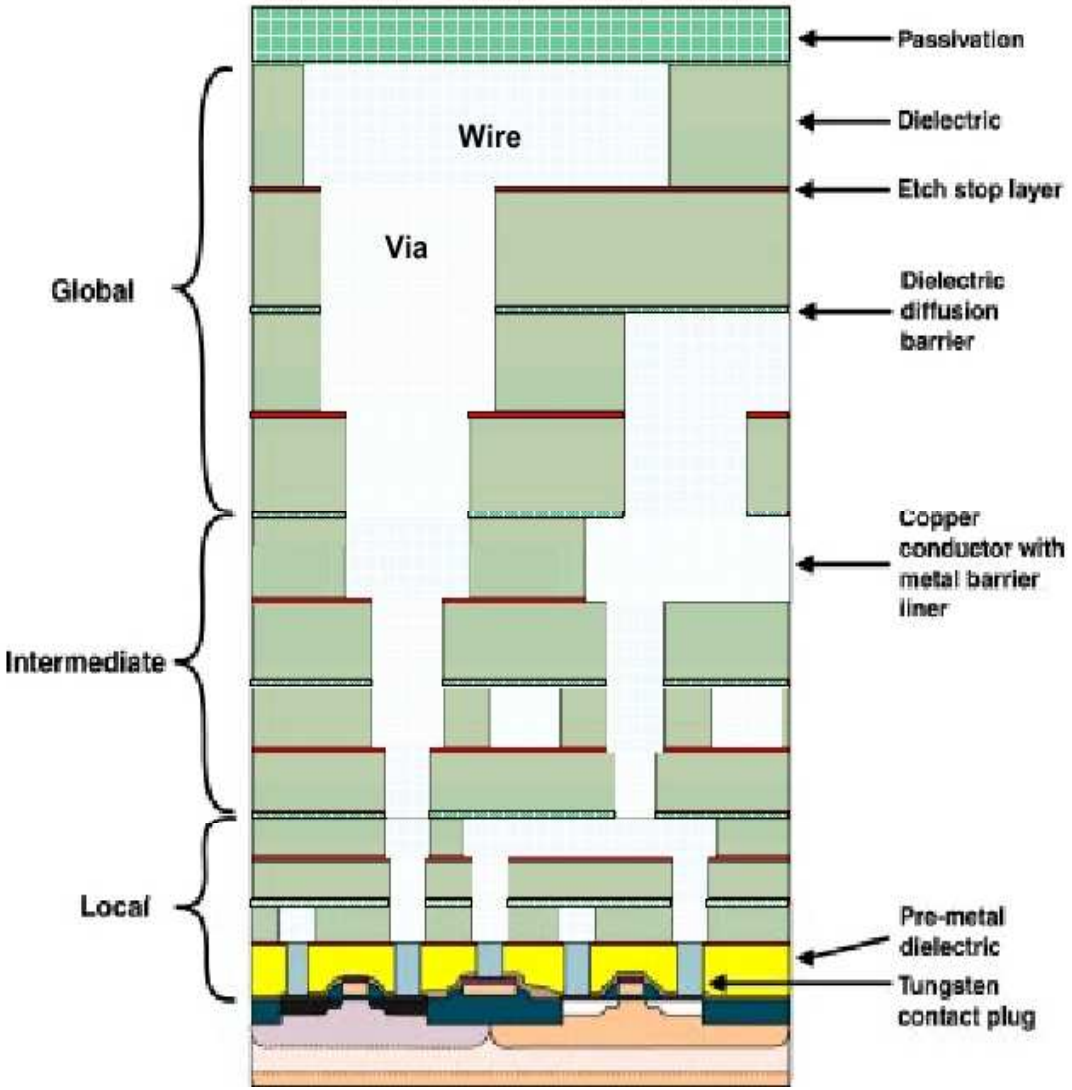
Cu-low k: state of the art
Future technology nodes

- **Variability**
  - Especially on levels with most aggressive design rules!
  - CMP: within die and within wafer non-uniformities
  - slight asymmetries in deposition techniques come on the foreground when technology is driven to its limit
  - k-value will be dependent on wiring level (because of different proximity of Si)
  - statistical control becomes important
  - CD control: line edge roughness ~ 10% of CD
  - Specific resistivity and k-value in narrowest dimensions

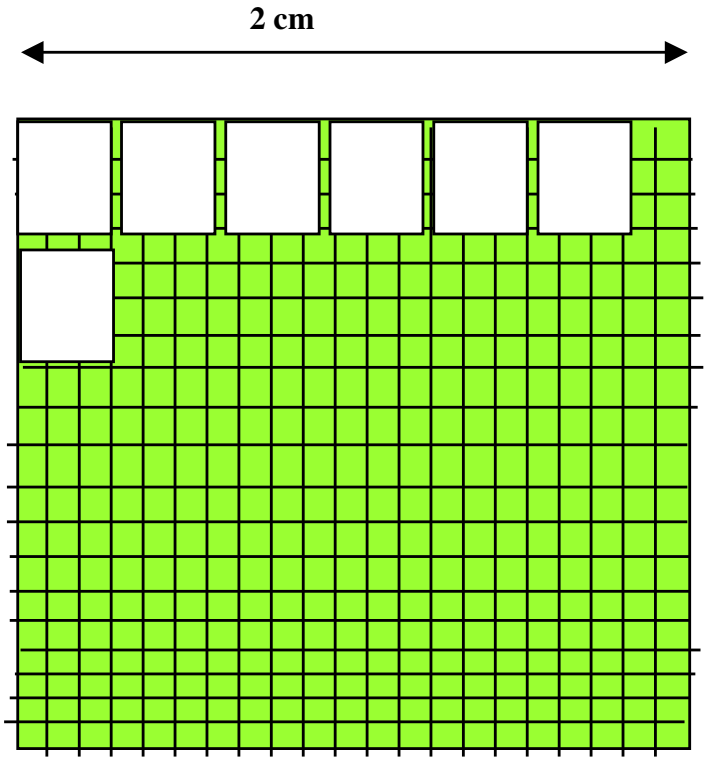
Cu-lowk: state of the art summary

- **Conclusion on the low k dielectric**
  - scaling k from 4.2 to 2.7 is a fact
  - scaling further from 2.7 to 2.0 is very difficult
    - more than 20 materials on the market, but none qualified
    - more materials to come
    - all are porous
    - porous materials are very difficult to process
  - there is a extensive collaboration between materials synthesis, equipment and users
  - there is an extensive effort in materials synthesis to provide the material with the right characteristics
  - solutions will come…cost for development is very high
- **Conclusions on the Cu: resistance for narrow lines will go up again**
- **Reliability and integrity will be a real challenge!**
- **Variability: real issue**

Wiring hierarchy



Wiring hierarchy



Local wires

Very short
Represent more than 90% of wire length

Intermediate wires

R = 300 - 500 Ohm/cm
l = 1 -3 mm
represent 9% of interconnects within functional blocks

Reference: IEEE proc. April 2001

Local/intermediate wires

	2004	2007	2010	2013
	90nm	65nm	45nm	32nm
ρeff [μOhm.cm]	2.2	2.2	2.2	2.2
pitch (local) [nm]	210	150	105	75
pitch (intermediate) [nm]	265	195	135	95
A/R [wire/via]	1.7/1.5	1.7/1.6	1.8/1.6	1.9/1.7
local frequency [MHz]	3990	6739	11511	19348
τnMOS-HP (ps)	0.99	0.68	0.39	0.22
τnMOS-LOP (ps)	1.84	1.14	0.85	0.56
		ρ_{eff} cannot be met!		

-effective resistivity specification cannot be met for future nodes

-definition: figure of merit for wires:

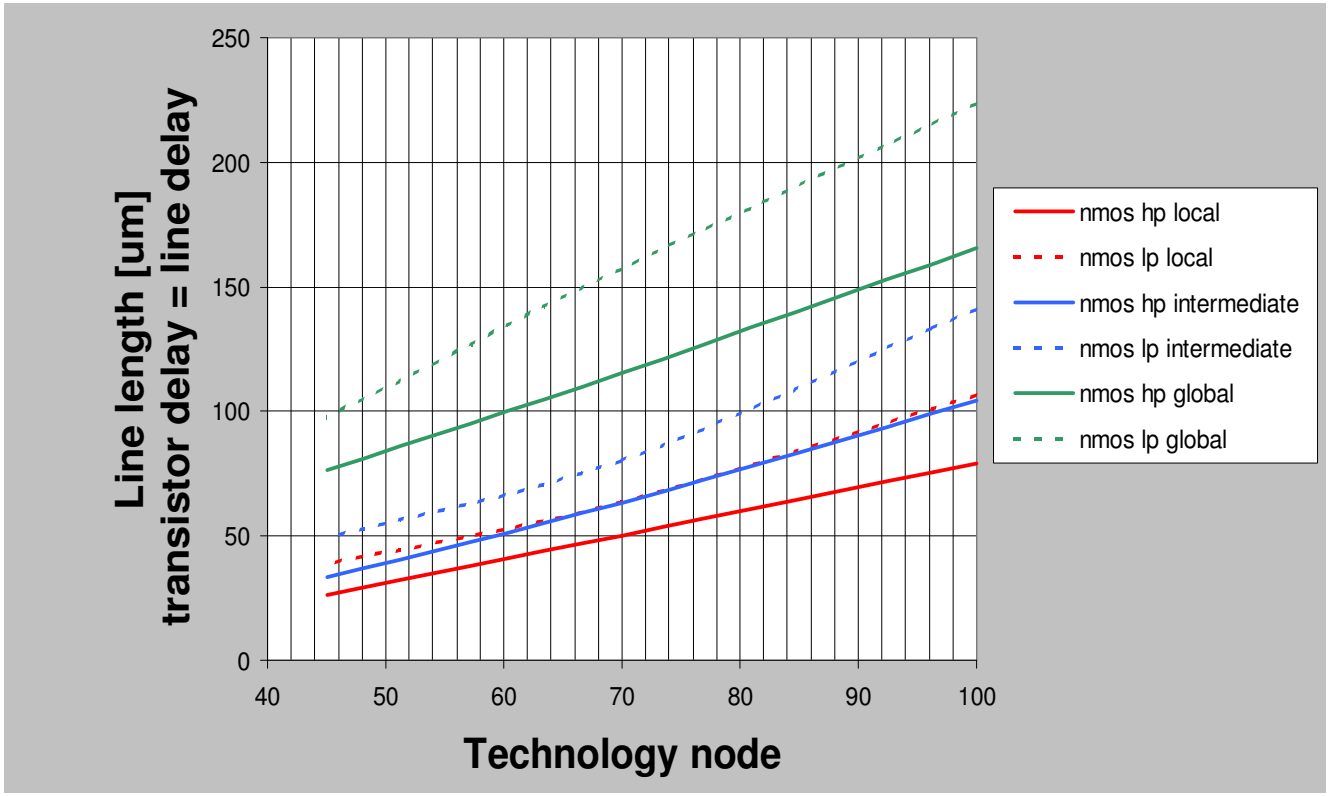
$$L \text{ for which } RC = C_{gate} \times V/I_{sat}$$

-how far can local and intermediate wires reach in 1 “local” clock cycle

Wiring hierarchy

- **Figure of merit for interconnect:**

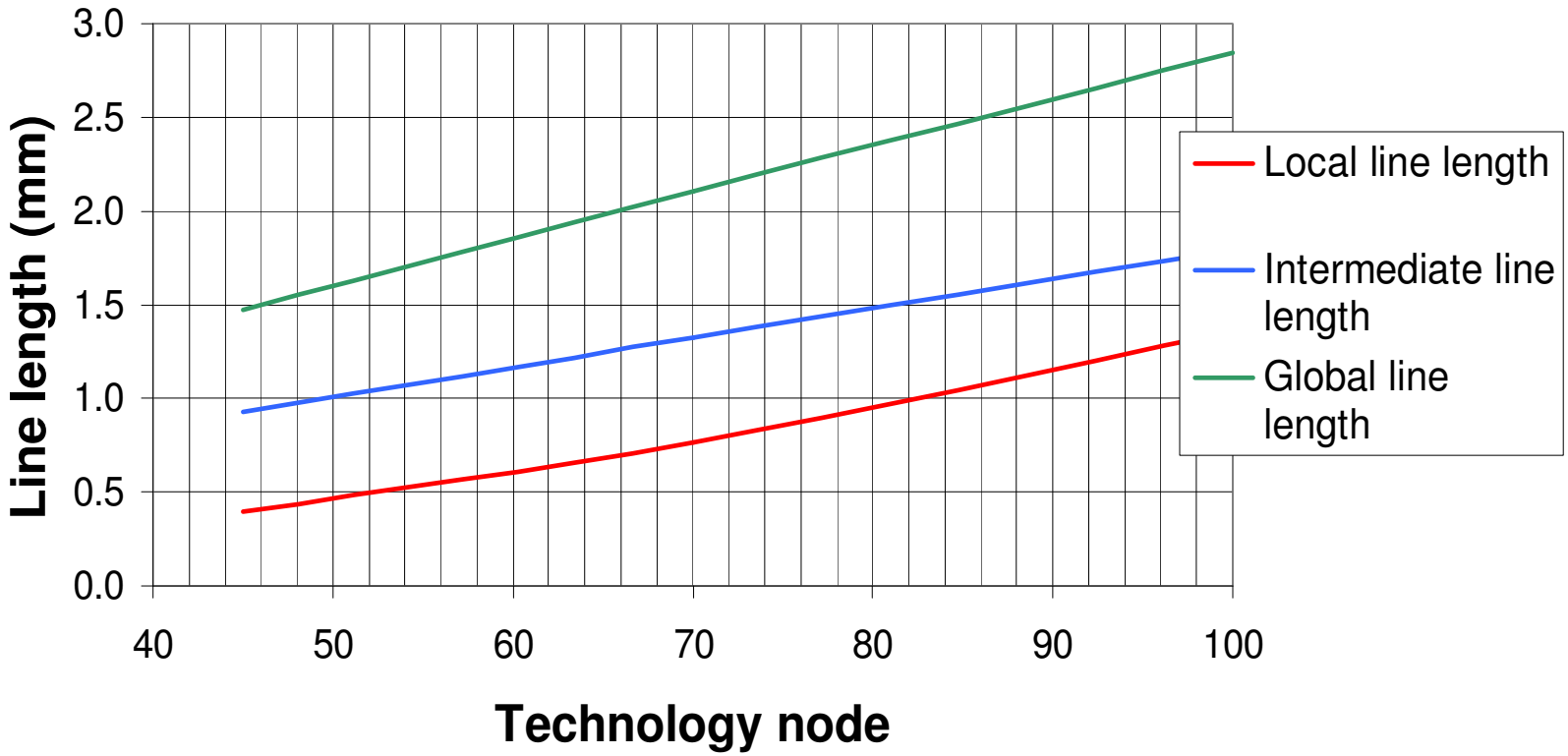
Length for which interconnect delay = transistor delay



- 25μm to 100μm for 45 nm node
- this is an optimistic view
- probably factor 1.5 to 3 smaller for local and intermediate wires

Wiring hierarchy

- **How far can signal reach in one local clock cycle (local frequency)**

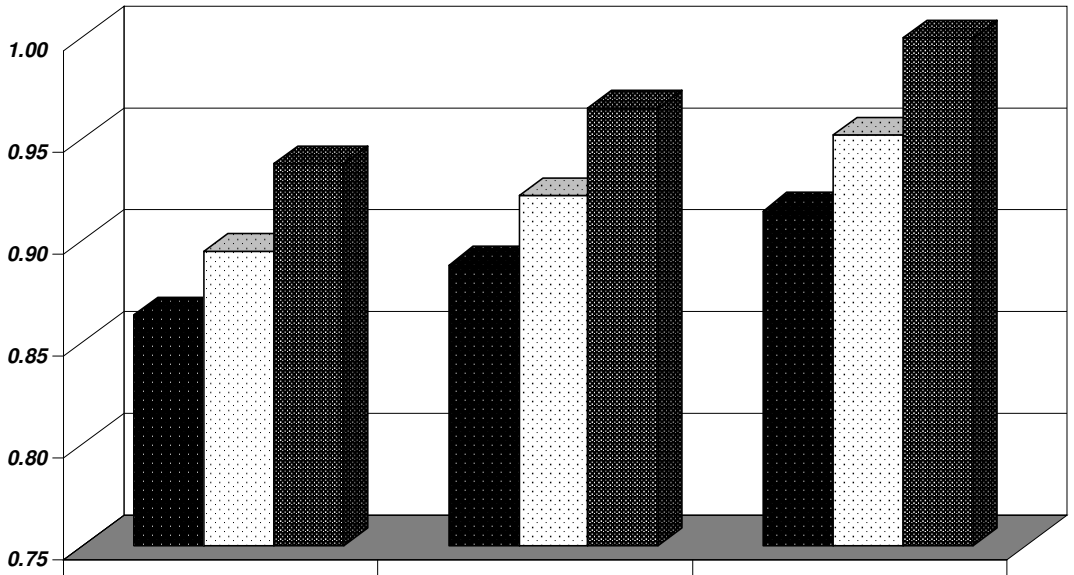


⇒1mm for 45 nm node, but will be factor 1.5 – 3 less
⇒What to do with functional blocks?

Wiring hierarchy

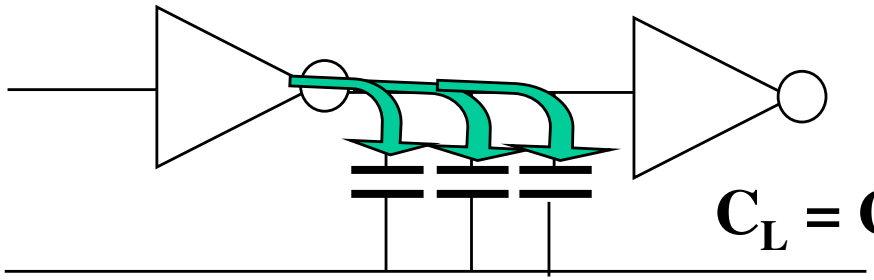
- **Effect of K on line length**

Line length relative to longest line (=lowest RC delay), local wiring, 65 nm node



	2.7	2.4	2.1
3.3/3.3/4.5	0.86	0.89	0.91
3.3/3.3/3.3	0.89	0.92	0.95
2.7/2.7/2.7	0.94	0.97	1.00

Wiring herarchy
Power issues



$$C_L = C_{out} + C_W + C_{Gi}$$

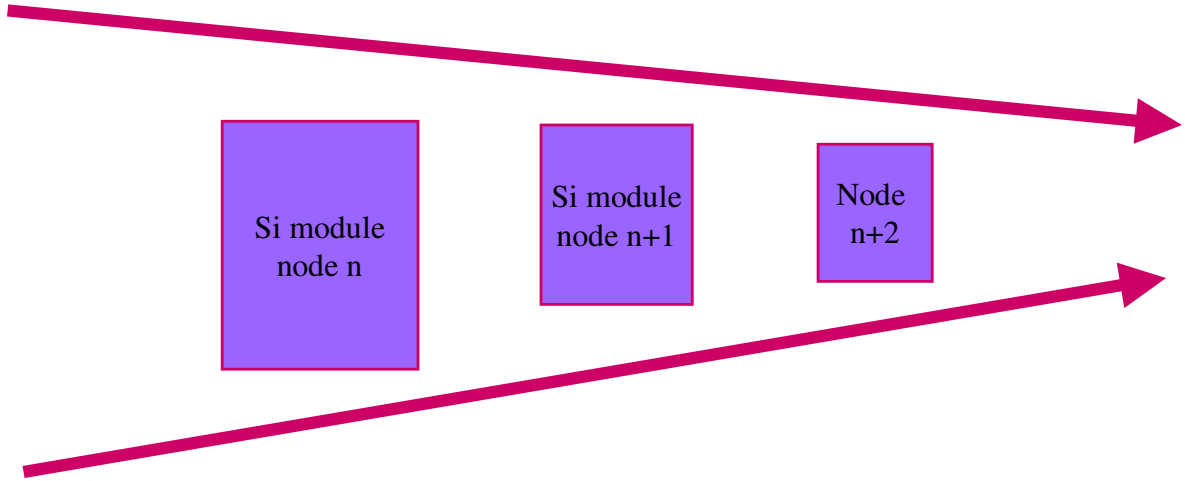
Drive current of the transistors has to charge all capacitors

Power=C_W. $V^{2.}$ f

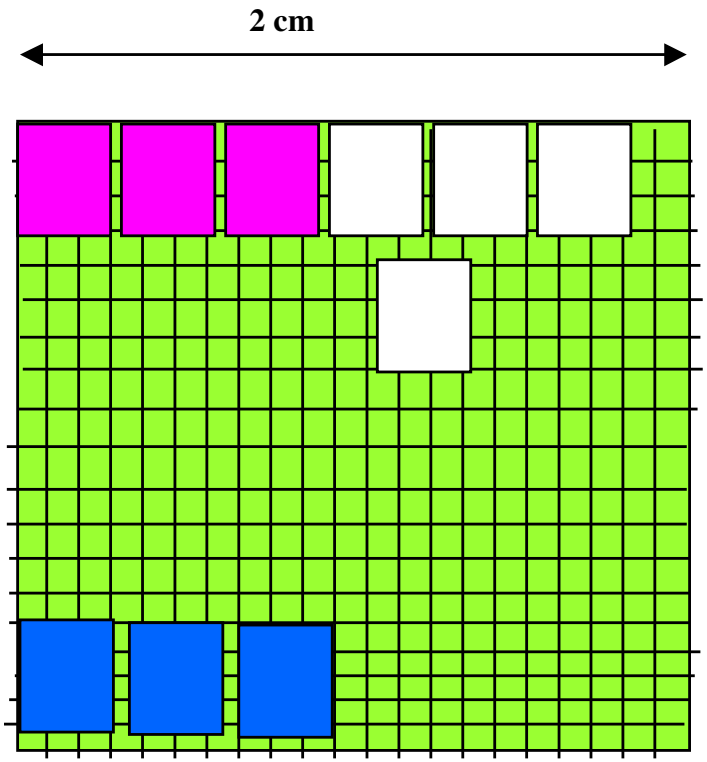
	2004	2007	2010	2013
	90nm	65nm	45nm	32nm
Local/intermediate				
total length [m/cm2]	6879	11169	16063	22695
local frequency [MHz]	3990	6739	11511	19348
Power/ active length [μW/μm]	0.6-0.8	0.6-0.8	0.6-0.8	0.6-0.8

Si modules

- Partitioning in micro-architectures down to physical design
- Si modules
  - can be designed with the traditional physical design tools
  - can be scaled for future technology nodes
  - beyond 45nm?
- Challenges for technology remain and are very well specified:
  - alternative conductors to deal with higher ρ_{eff} for narrow wires
  - electromigration
  - use of low k dielectrics in very narrow spacings
  - process variations



Wiring hierarchy

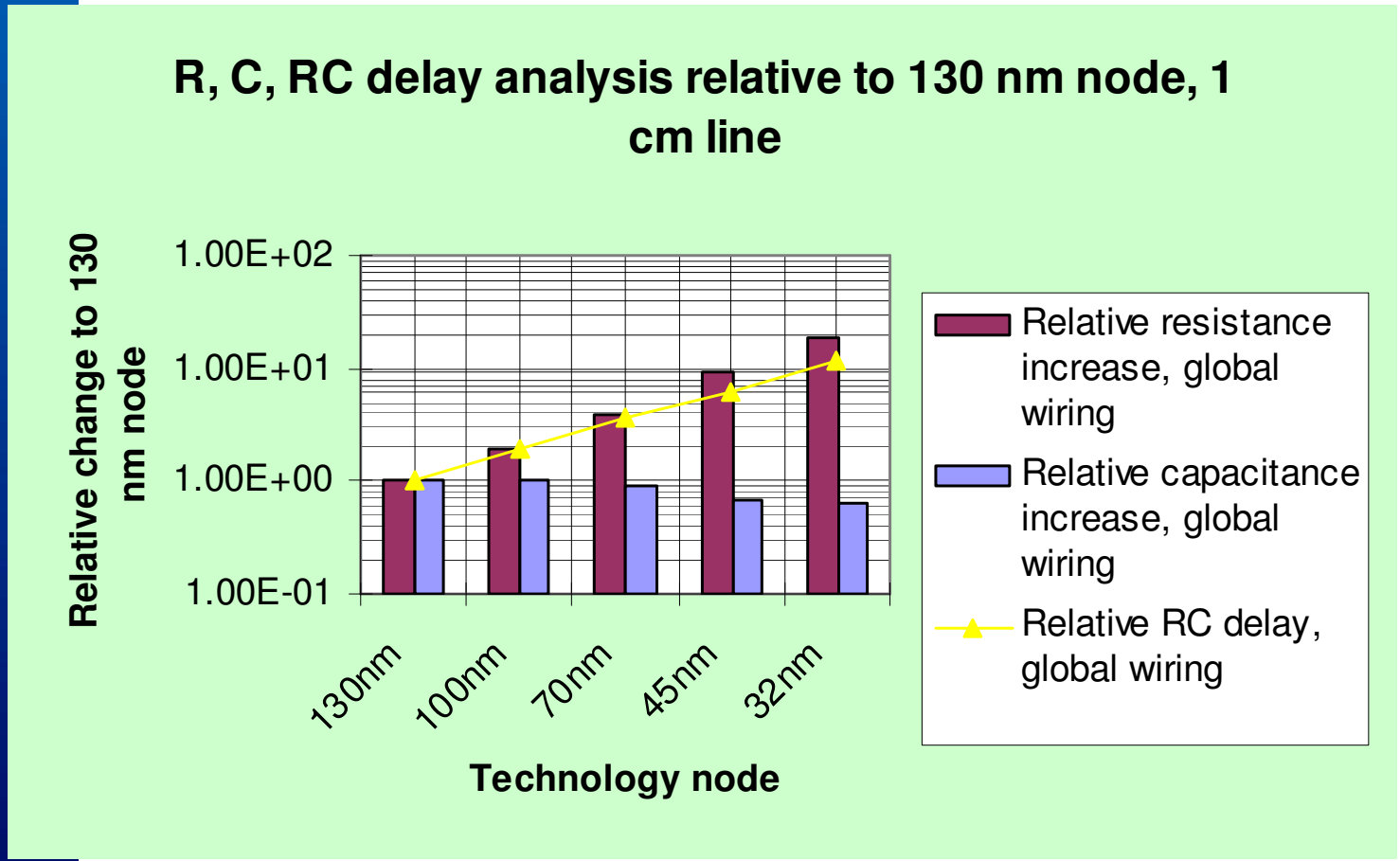


Global wires
- >5mm
- represent 1% of total interconnects
- synchronous modules in an asynchronous sea

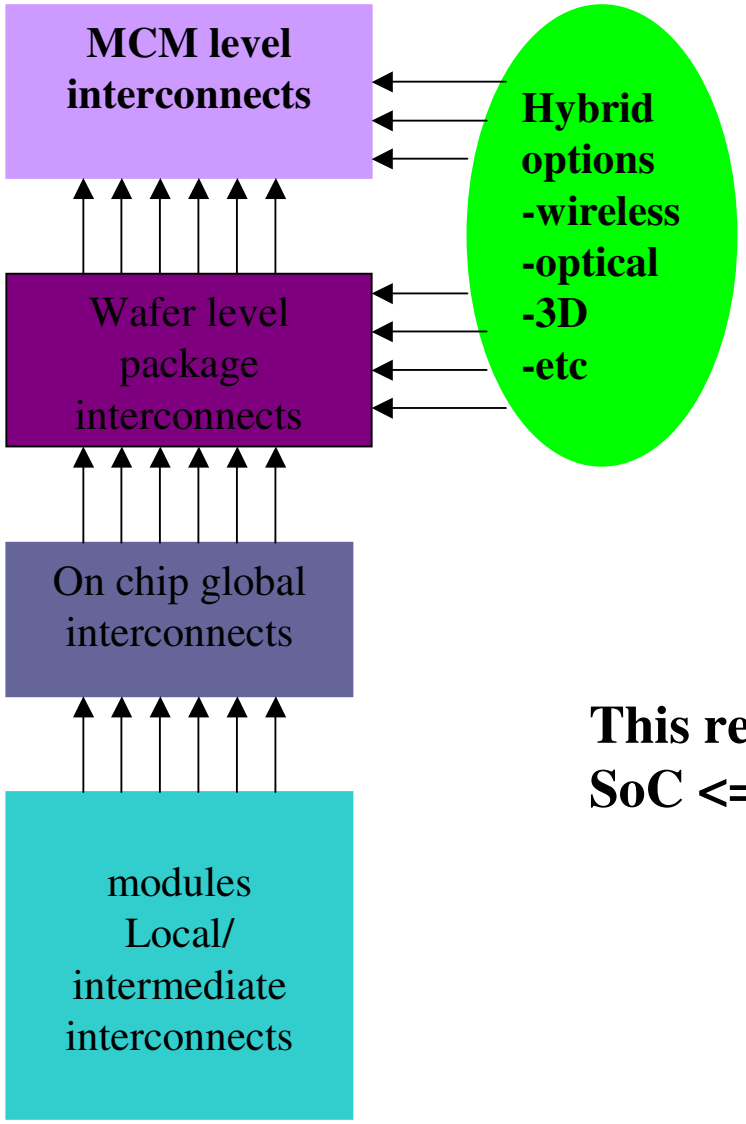
From IEEE proc. April 2001

Global wiring

	2004	2007	2010	2013
	90nm	65nm	45nm	32nm
ρeff [μOhm.cm]	2.2	2.2	2.2	2.2
min. pitch [nm]	460	290	205	140
chip size [mm2]				
MPU	140	140	140	140
MPU/ASIC	310	310	310	310
ASIC	572	572	572	572
SoC clock frequency [MHz]	300	450	600	900



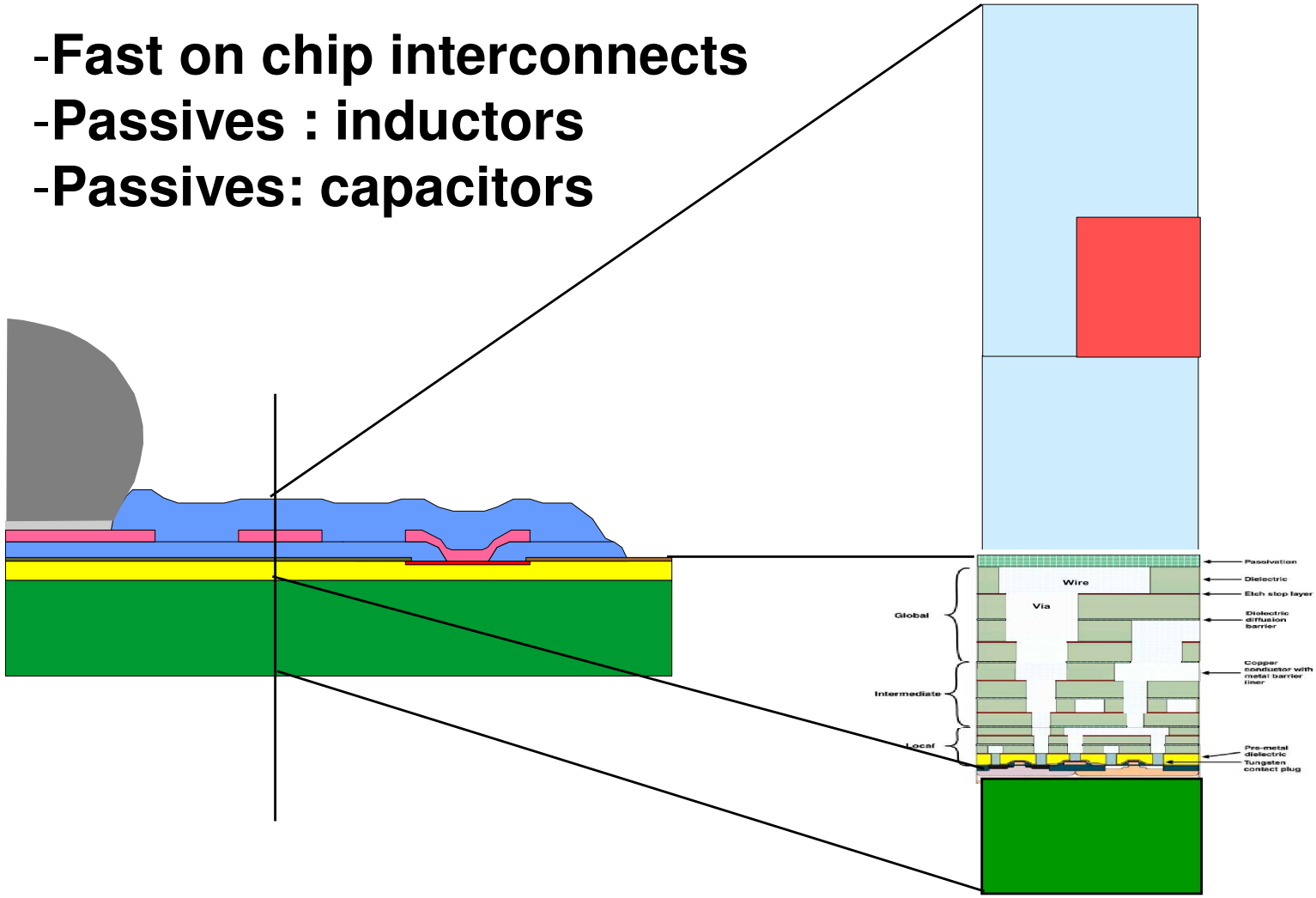
Wiring hierarchy



This relates to the SoC <=> SiP discussion

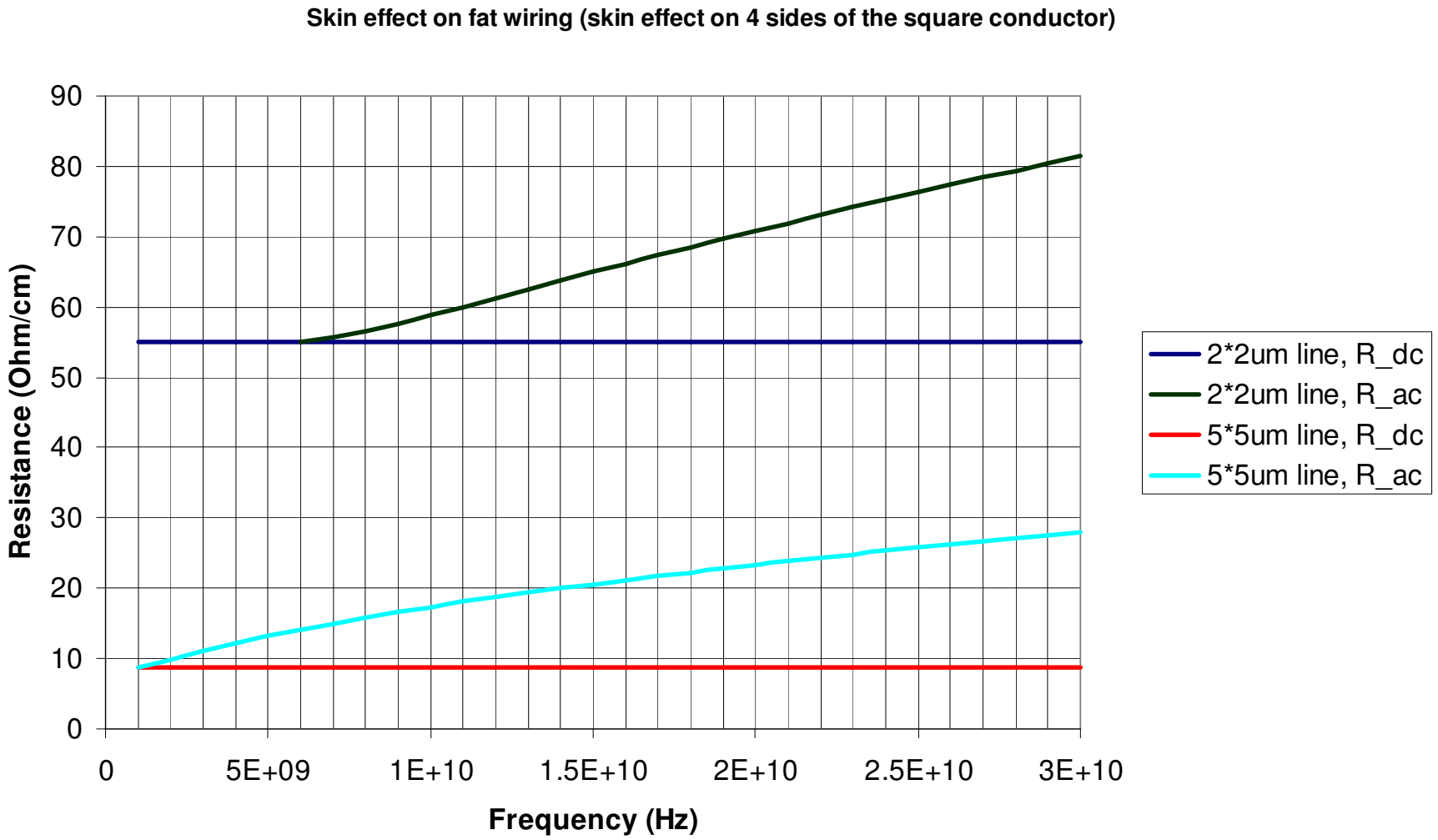
Extended wiring hierarchy
Redistribution Layer Interconnects

-Fast on chip interconnects
-Passives : inductors
-Passives: capacitors

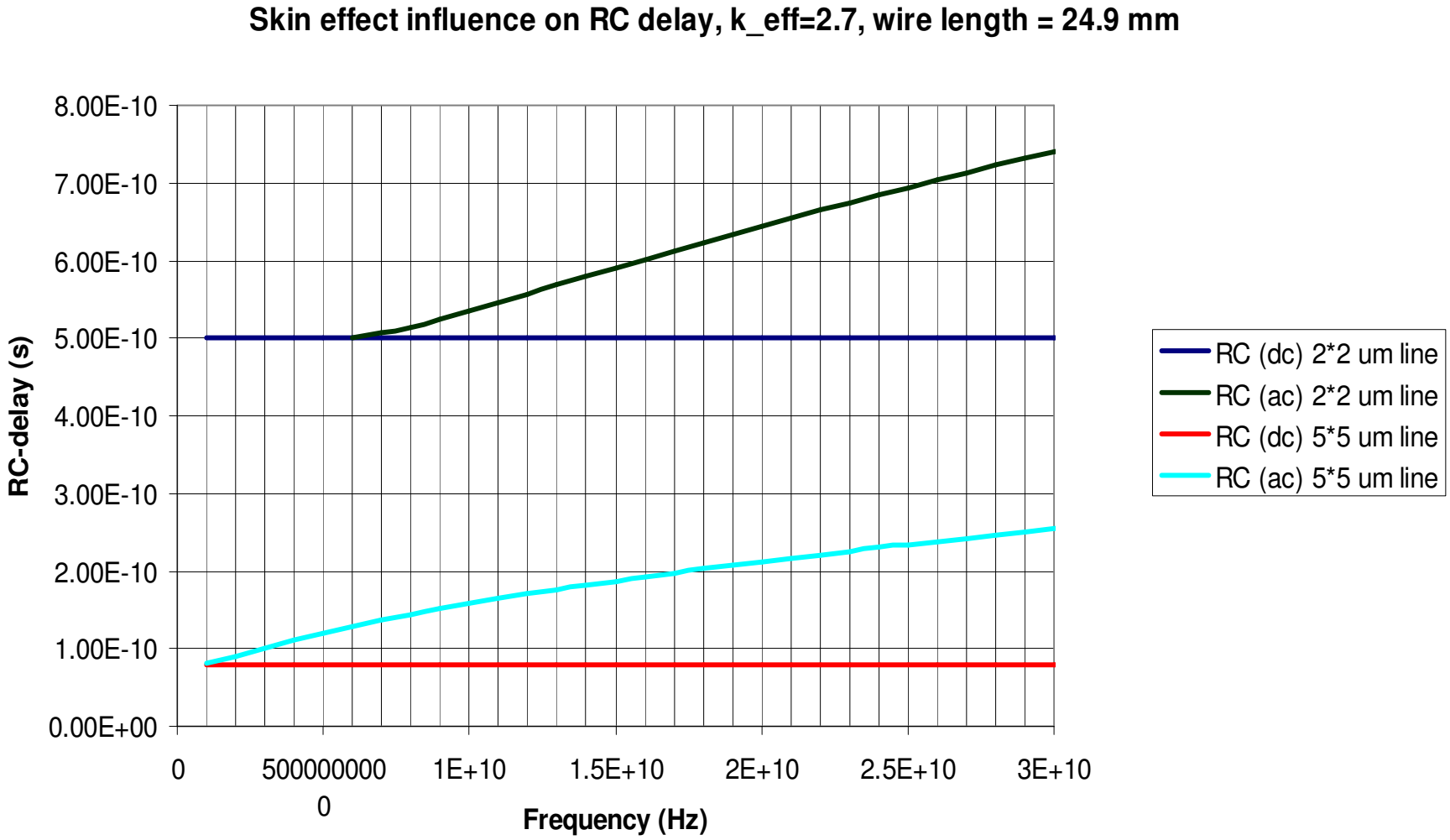


Ref. Eric Beyne, IMEC

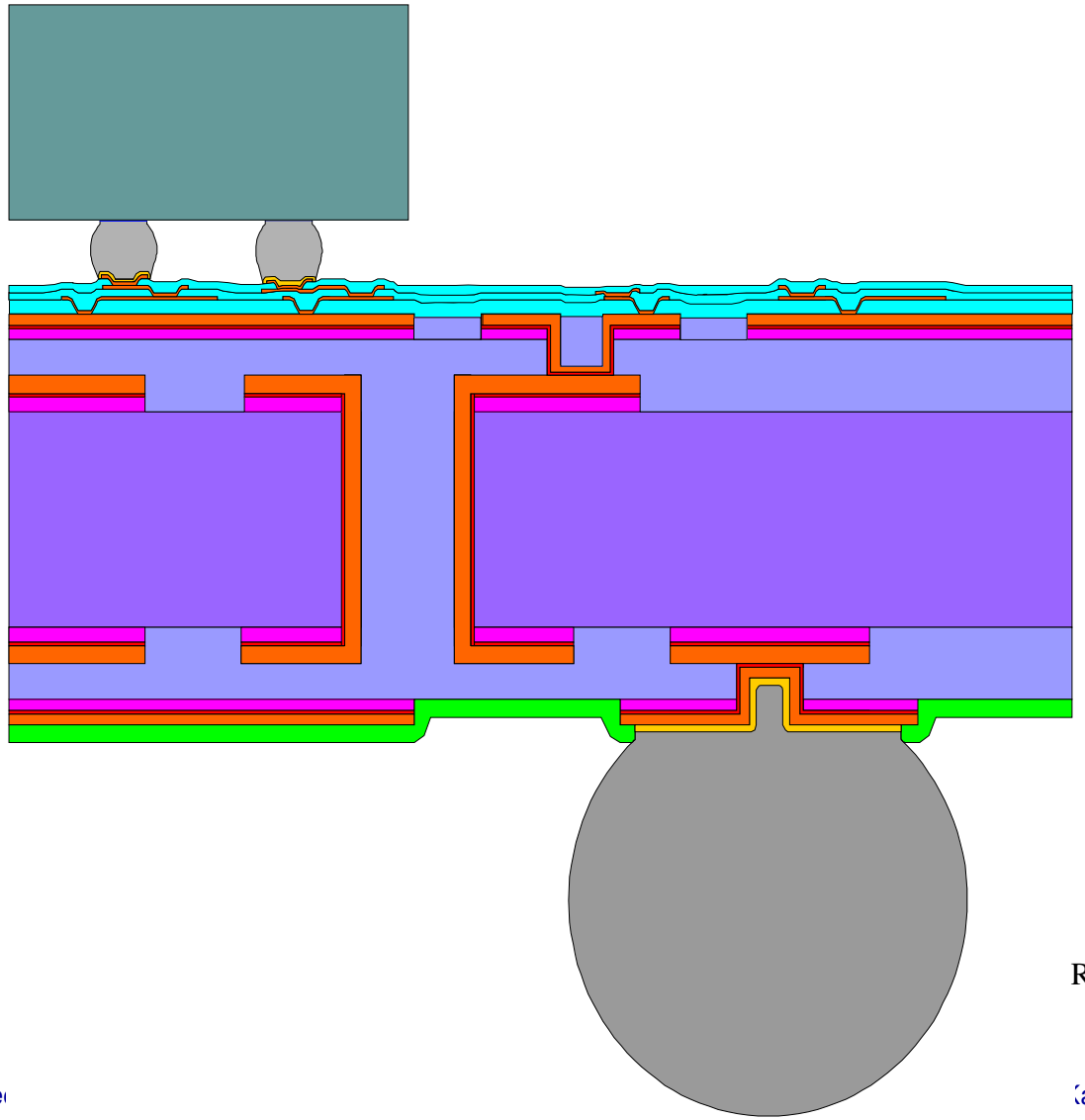
Estended wiring hierarchy wafer level package routing



Extended wiring hierarchy wafer level package routing

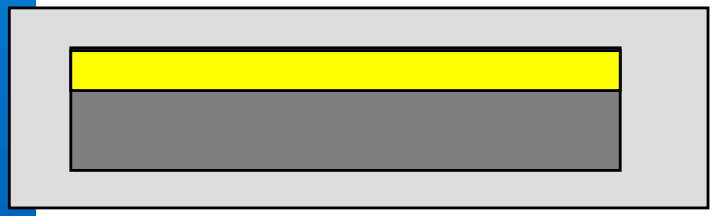


Extended hierarchy: exterconnects
Thin film deposition on laminate : MCM L/D

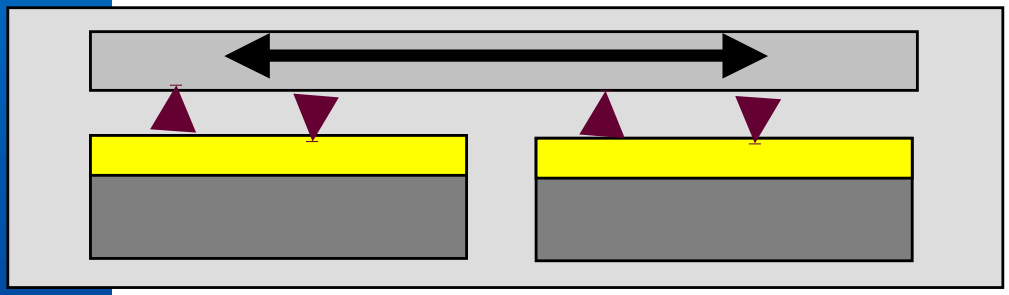


Ref. Eric Beyne, IMEC

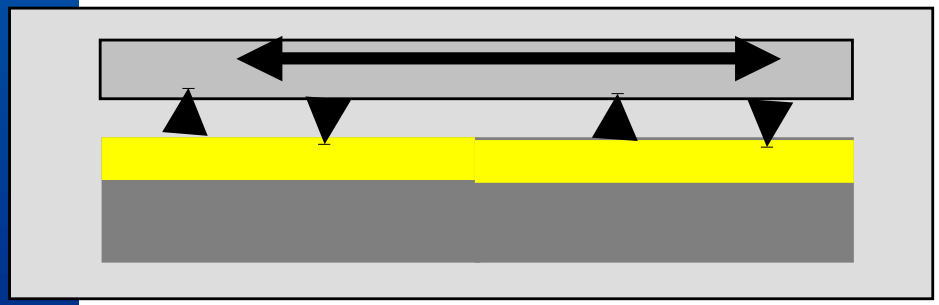
SoC versus SiP



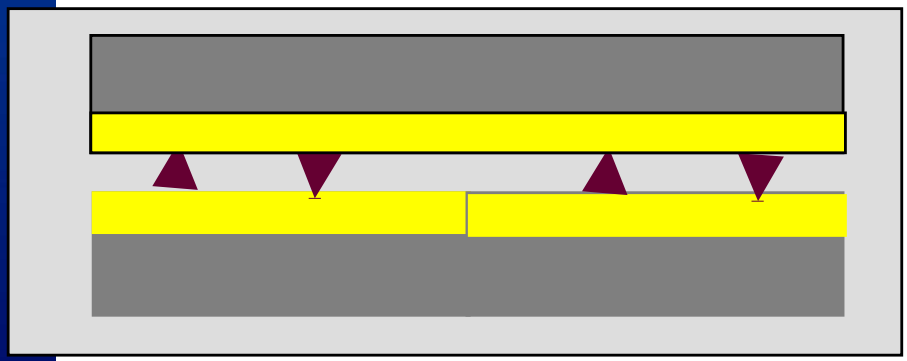
SoC: advanced technology
Si modules+ global wiring + wafer level package



SiP: several chips/hybrid communication



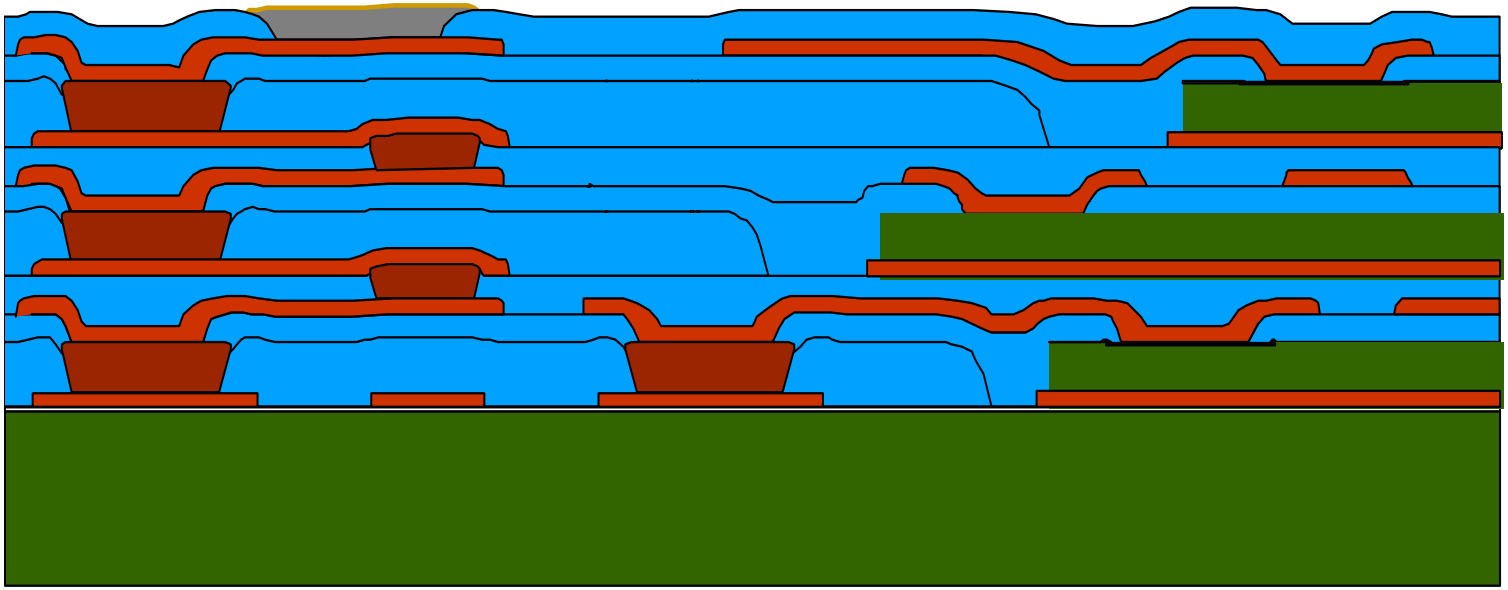
SoC: hybrid global wiring



SoC/SiP:
data communication on upper chip
computing/storage on lower chip

Extended wiring hierarchy: 3D- MCM-D : Ultra Thin Chip Stacking (UTCS)

Very thin die (10 μm), embedded in a MCM-D multilayer structure



Ref. Eric Beyne IMEC

Intermediate conclusions

- **Partitioning of chip based on local/intermediate and global wiring leads to very small Si modules**
- **Wiring hierarchy can be extended**
  - Local/global wiring
  - Wafer level package wiring
  - SiP combinations
  - Exterconnects/3D chip stacks etc
- **Global wiring can be addressed with these new interconnect schemes**
- **Still there is a lot to be optimized for on chip local/intermediate interconnects**

Case study: memory design

Can we exploit interconnect technology to power and/or speed problems

Software tool based on Pareto analysis: optimization of choices available

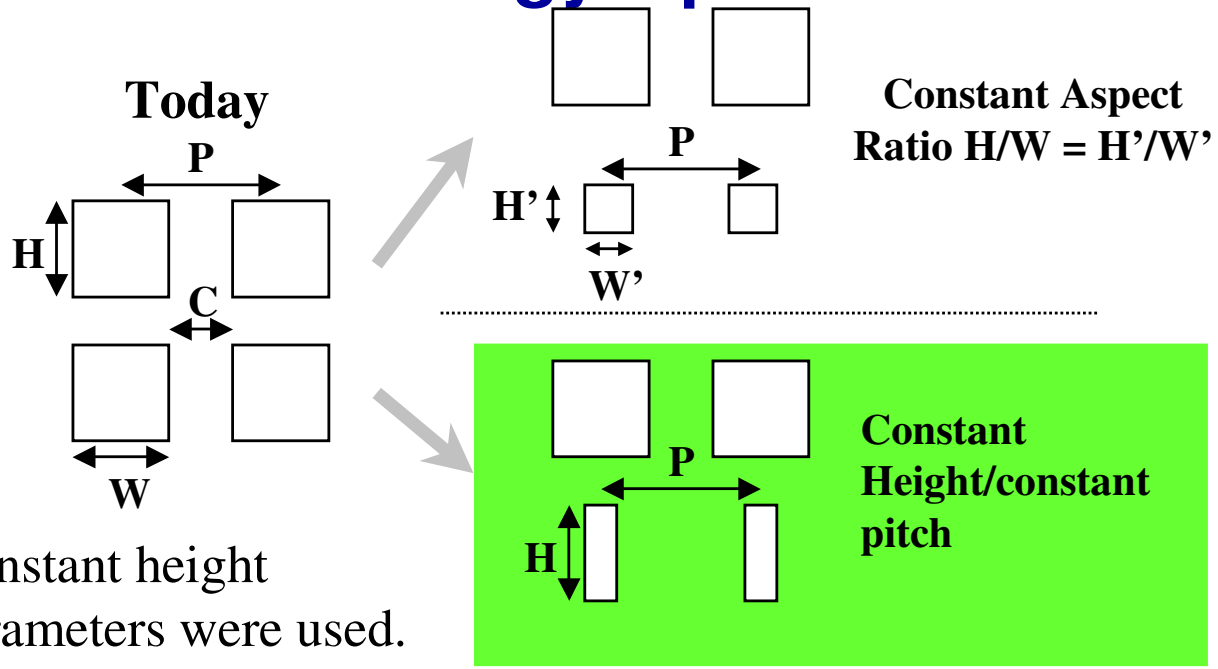
Example: application specific design: SRAM

=>Pareto exploration:

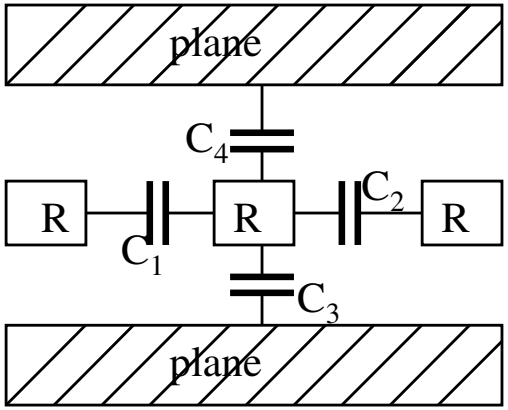
- **"realistic" modifications in technology**
- **V_{dd} as parameter**
- **8Kbit (1k x 8) SRAM**
- **50nm technology node**

To find out whether a proposed technology parameter is important in optimizing the complete system

Case study
Technology Options for Interconnect

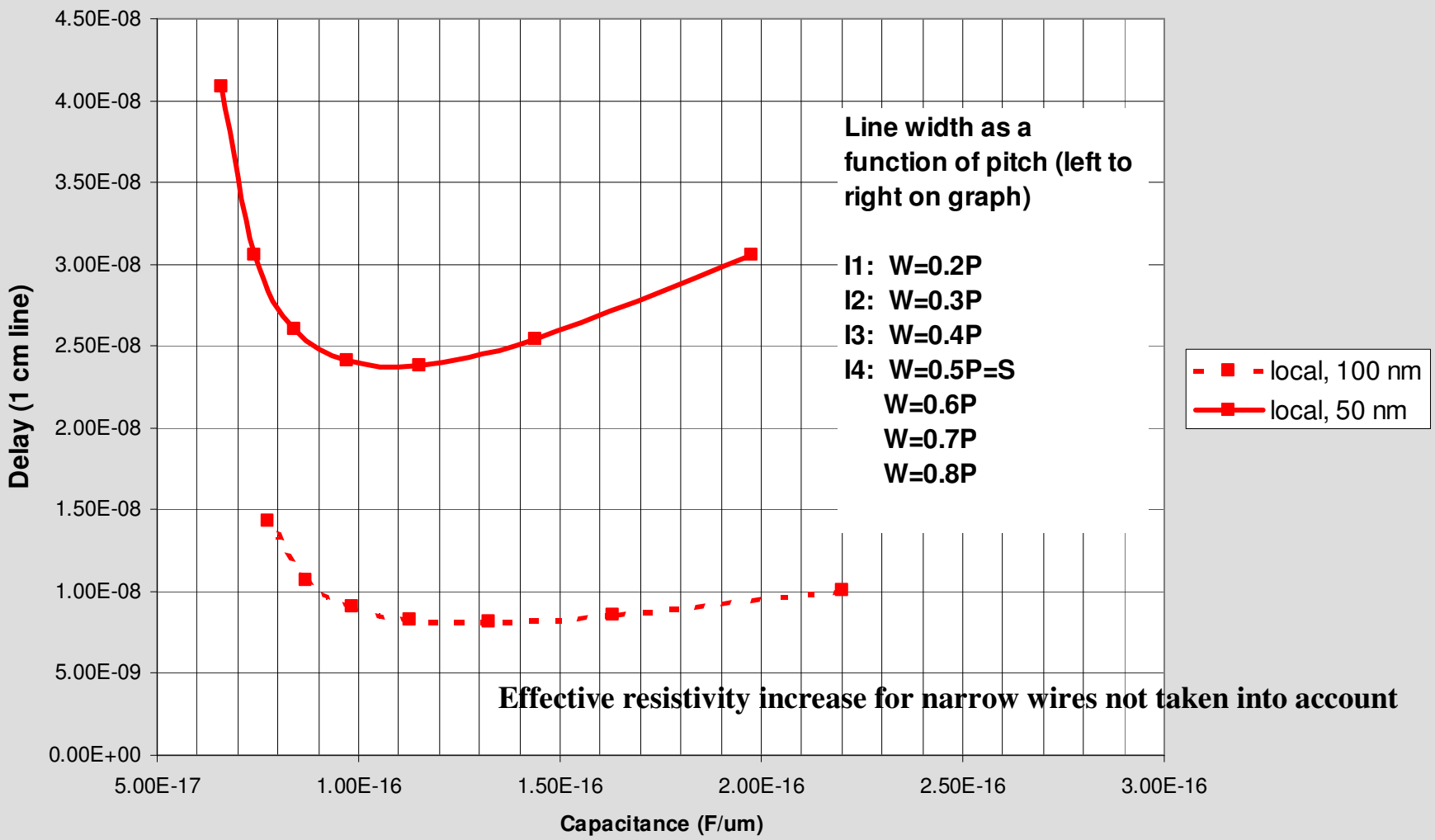


Constant height parameters were used.

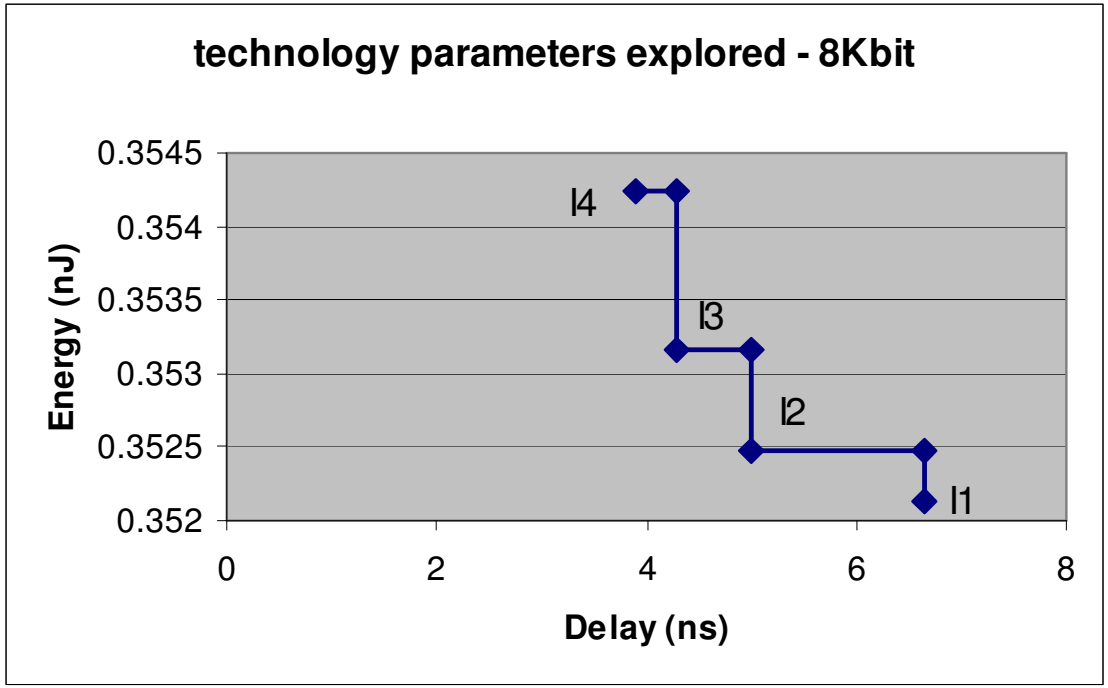


Total capacitance is the sum of the different capacitances. (model)

Case study
definition of interconnect parameters



Case study
Pareto Exploration Interconnect Parameters



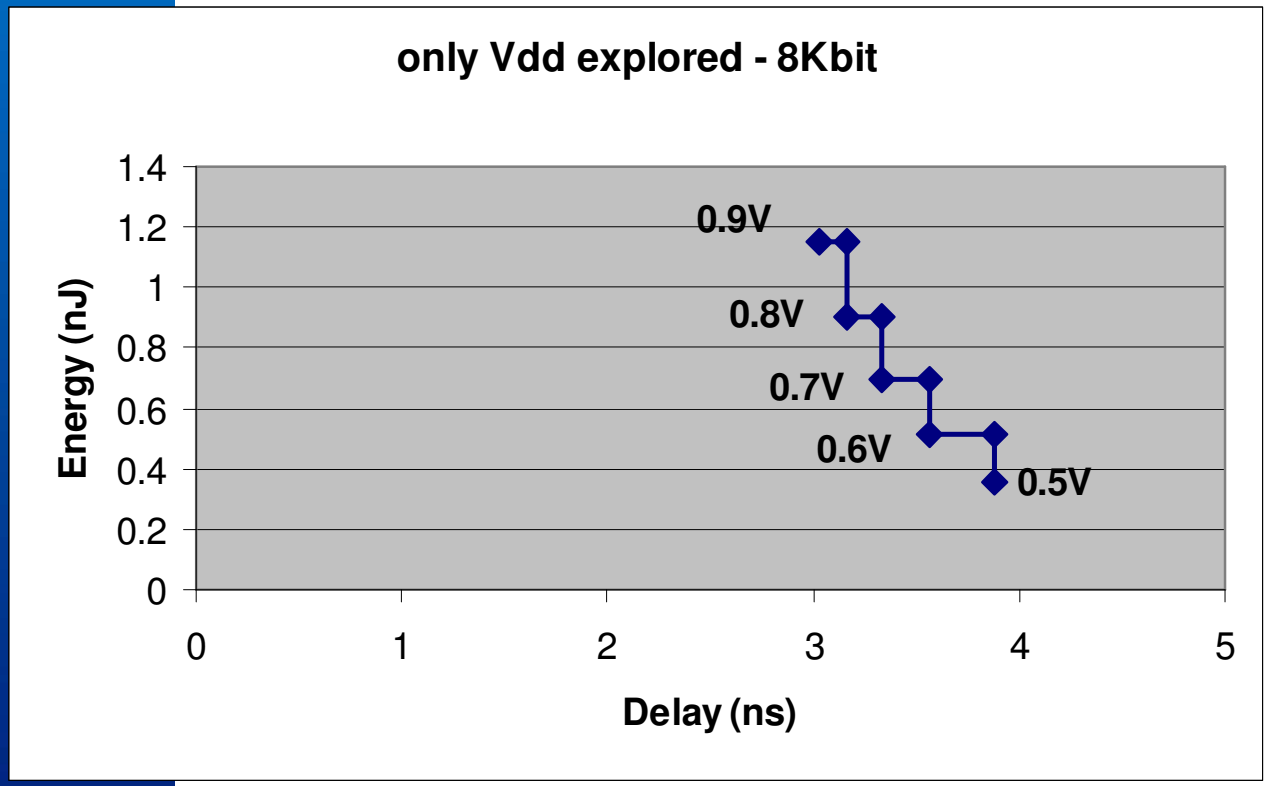
Assumptions:

- V_{dd} = 0.5V
- 1k x 8 SRAM
- 50nm tech node
- I4 is the fastest interconnect
- I1 is the slowest interconnect

Exploring interconnect parameters mainly affects delay.

The impact on energy consumption is very small.

Case study
Pareto Exploration of V_{dd}

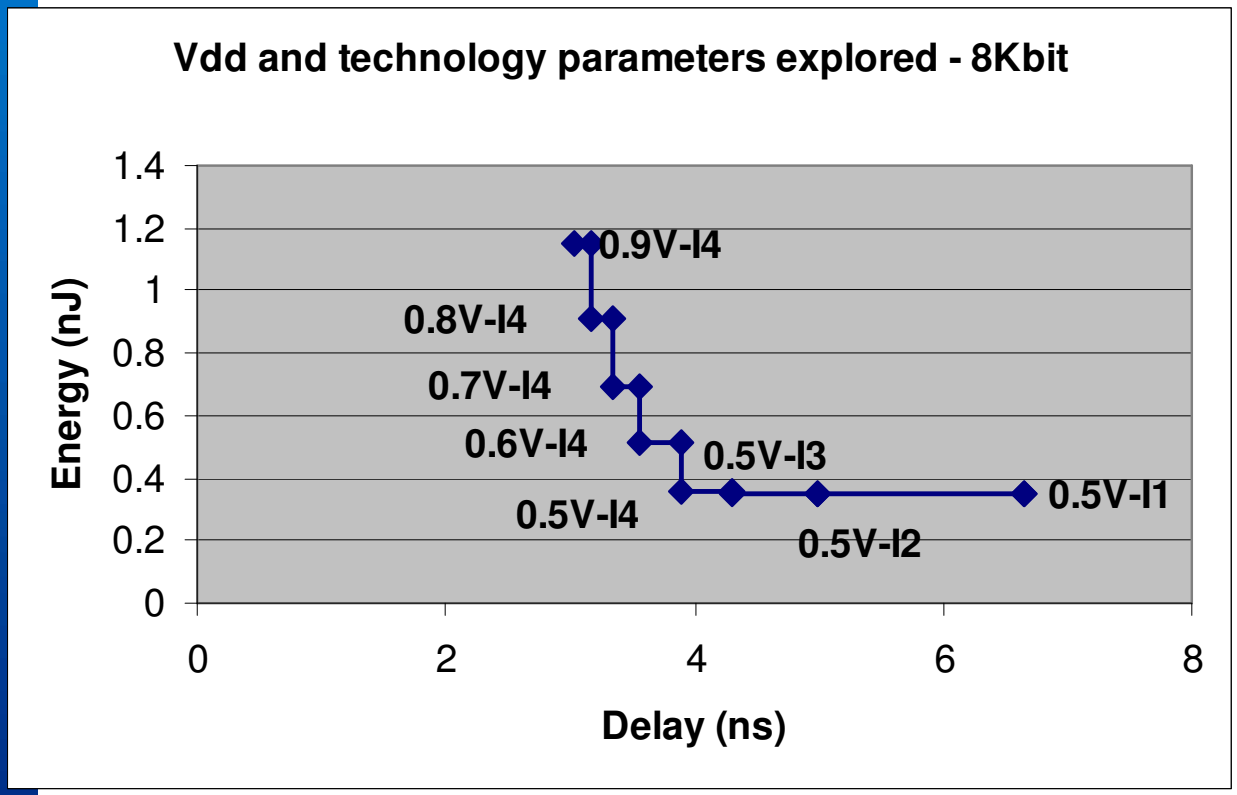


Assumptions:

- fast interconnect
- 1k x 8 SRAM
- 50nm technology node

V_{dd} scaling has a major impact on energy consumption and a smaller influence on delay.

Case study

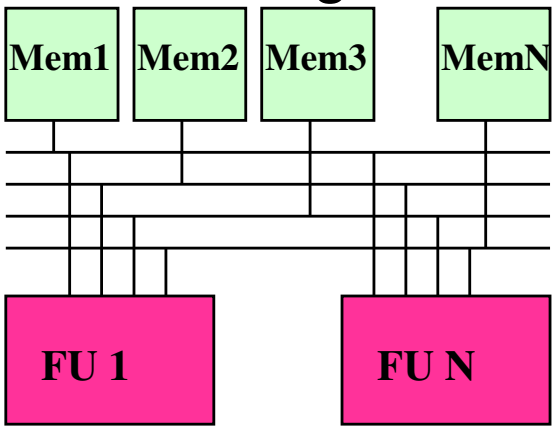


- 8Kbit (1k x 8) SRAM
- 50nm technology node

- The Pareto points cover a wide range both in power consumption and in delay.
- Many are in the "optimal" region, having small delay and power consumption, but there are sufficient points to cover the other regions for global system wide trade-offs.

Case study
Modeling the inter memory interconnect

Floorplan for an entire design.



Each memory has its own bus. The bus' width is equal to the memory bitwidth.

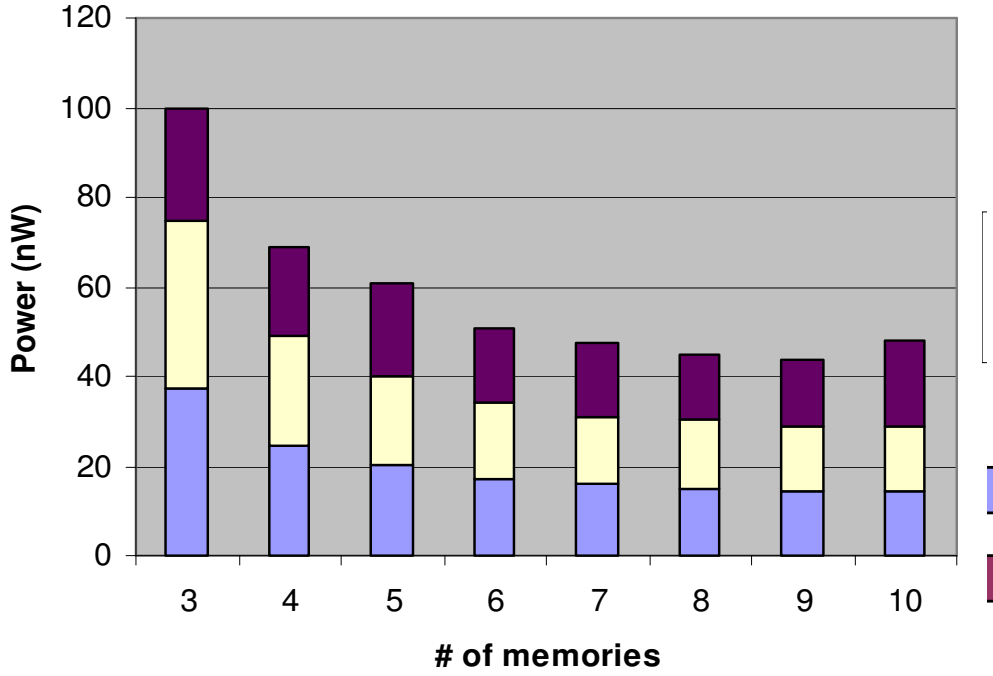
Functional units are connected to every bus.

The length of the buses is equal to the sum of the memory widths.

Only the buses and not the connection from the memories and the FUs to the buses are considered for power estimation.

Lengths of inter- and intra- memory interconnect are comparable.

Case study:experiments on DAB Impact of Inter-Memory Interconnect



Assumptions:

- V_{dd} = 1V
- fast tech parameters
- 9ns target delay

Inter and intra-memory interconnects follow the same trend for energy consumption

Inter memory interconnect power is about 30% of the total power consumed

We canmatch the architecture to the application

Technology development Cost

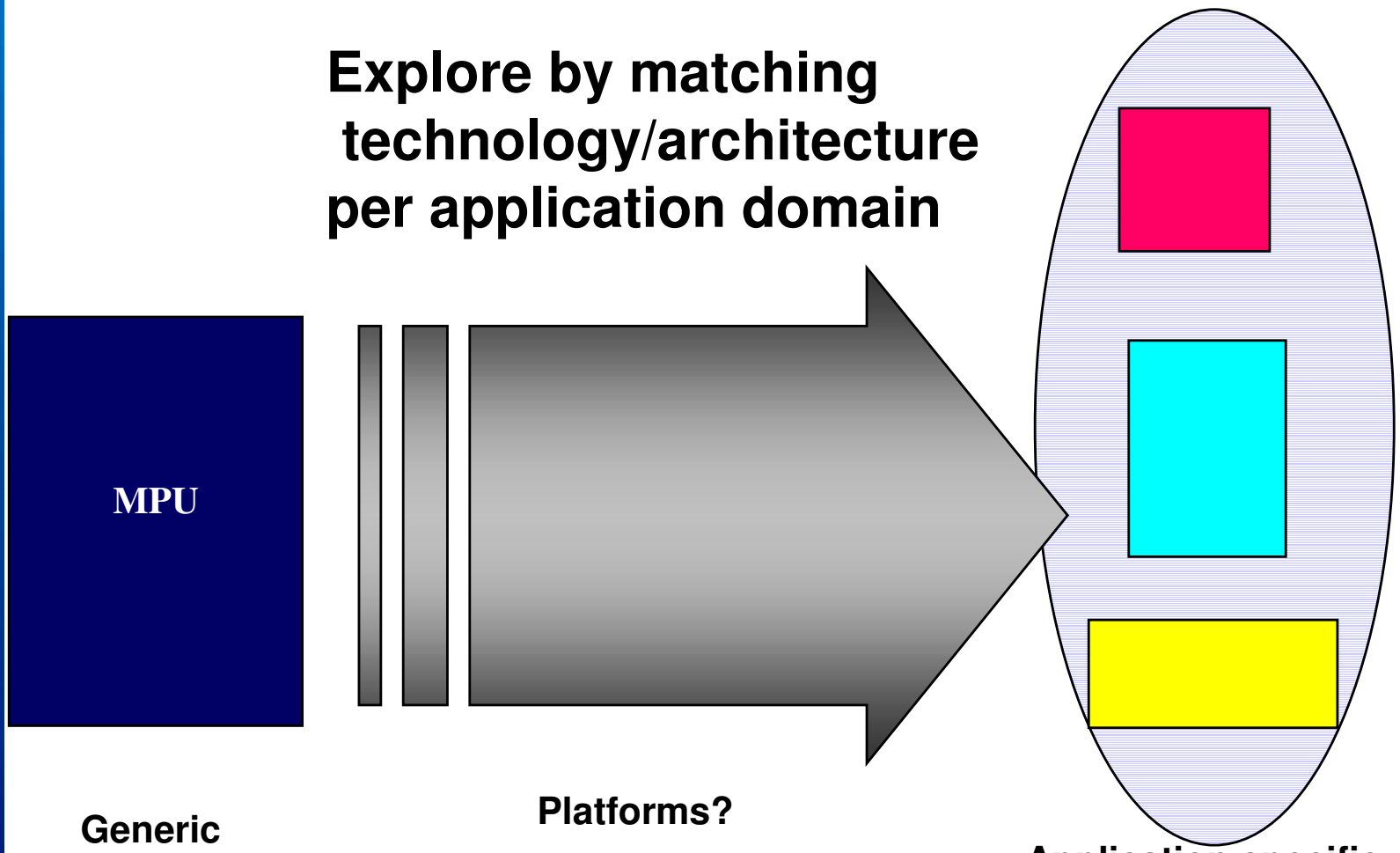
- **Face some facts:**
  - 300 mm: Si area on chip becomes cheaper

    area x 2, process x 1.3 (as compared with 200mm)
  - masks become very…expensive: strong wish for maskless patterning from foundries
  - equipment development is oriented towards high end applications
  - technology development/optimization becomes mask dependent

- **Questions:**
  - **re-use of design and technology**
  - **re-use of process step development/equipment development**
  - **re-use of masks**
  - **limiting verification**

Interconnects and platforms

Explore by matching technology/architecture per application domain



Conclusions and final questions

- **Complexity of technology development is enormous**
- **Can we partition problems to better solve them?**
  - Design modules that can be handled by current/future software tools including physical models and interconnects
  - Develop/optimize technology for these modules and concentrate on the technological challenges
  - Reuse the design and technology of these modules
  - Develop technologies for wiring these modules (global level/wafer level package/hybrid technologies either on chip or in various package concepts)
  - Match this technology methodology with system design methods:use same partitioning
  - Develop design tools with a granularity of Si modules?

Workshops

- **IMEC is organizing discussion workshops for system designers and technologists**

“Interconnect Hierarchy: Technology and system design”

  - April 24, 2002
  - October 11, 2002

- **An initiative of**

  - Interconnect technology: Karen Maex
  - Packaging : Eric Beyne
  - System design: Francky Catthoor, Henk Corporaal and Hugo De Man