Analysis of High-Performance Clock Networks with RLC and Transmission Line Effects

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Outline

- Problems with present models
- Review of common models
- Clock Synthesis
- Results

Problems with Present Models

- The most prevalent model is the Elmore delay model, a first order RC delay.
  - At high frequencies the inductance of the lines plays a greater role.
- Many better models have been proposed but have only be used in analysis on uniform structures such as H-Trees
  - Modern design does not use such simplified design.

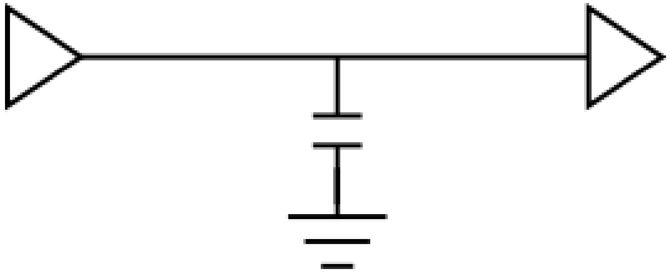
Problems with Present Models

- High-frequency designs now use clock grids which require substantial routing resources and large drivers consuming a great deal of power.

- In exchange for these design losses, skew and jitter are amortized across the chip and manufacturing error is more tolerable

Review of common models

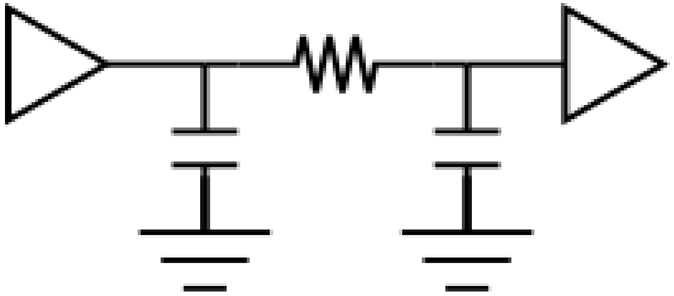
- Lumped C model
  - For short local wires the capacitance of the wire is the most dominating factor, and it is reasonable to assume that the resistance and inductance are negligible



- RC Model (Elmore model)

$$Delay = RC = (R_{unit} * L / W)(C_{unit} * L * W)$$

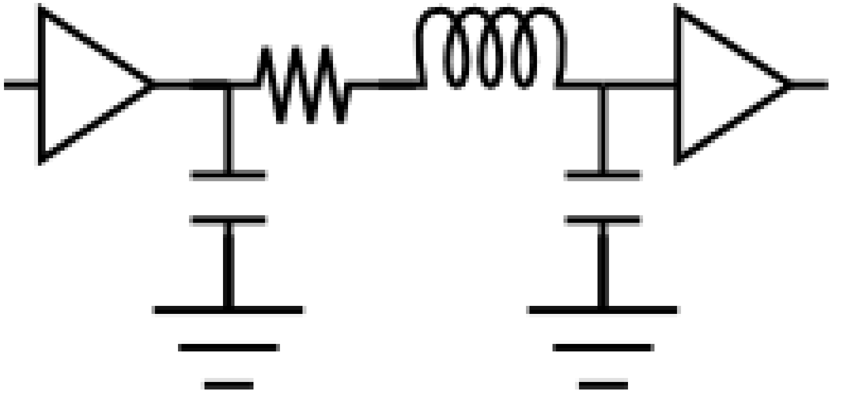
$$= R_{unit} * C_{unit} * L^2$$



  - Overestimates downstream capacitance
  - This error grows the larger the number of steps from the root

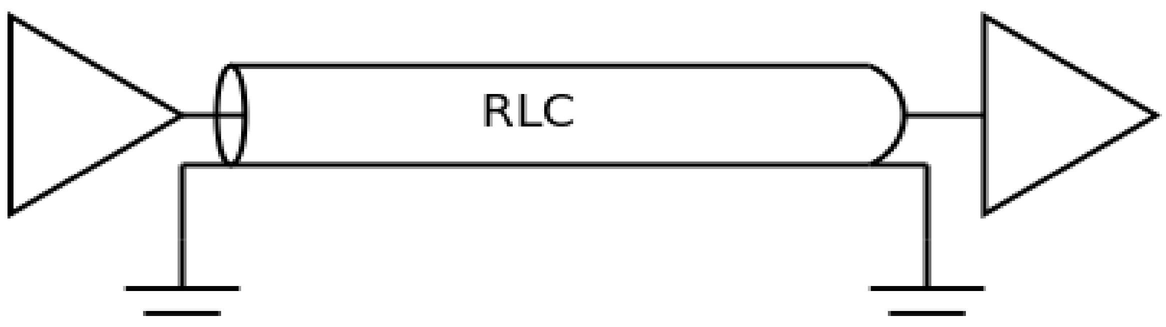
Review of common models

- RLC Model
  - On-chip inductance has long been ignored based on it's perceived insignificance due to the short wire lengths on IC.
  - However, as the frequencies have increased this becomes increasingly important particularly on the longer clock-lines.



Review of common models

- Transmission Line Model
  - The most accurate of the models.
  - Considers the knee frequency, defined as $0.5/t_{rise}$
  - Propagation velocity changes based on the frequency component of the signal
  - A 7.5GHz signal could easily have relevant spectral components exceeding 37.5GHz

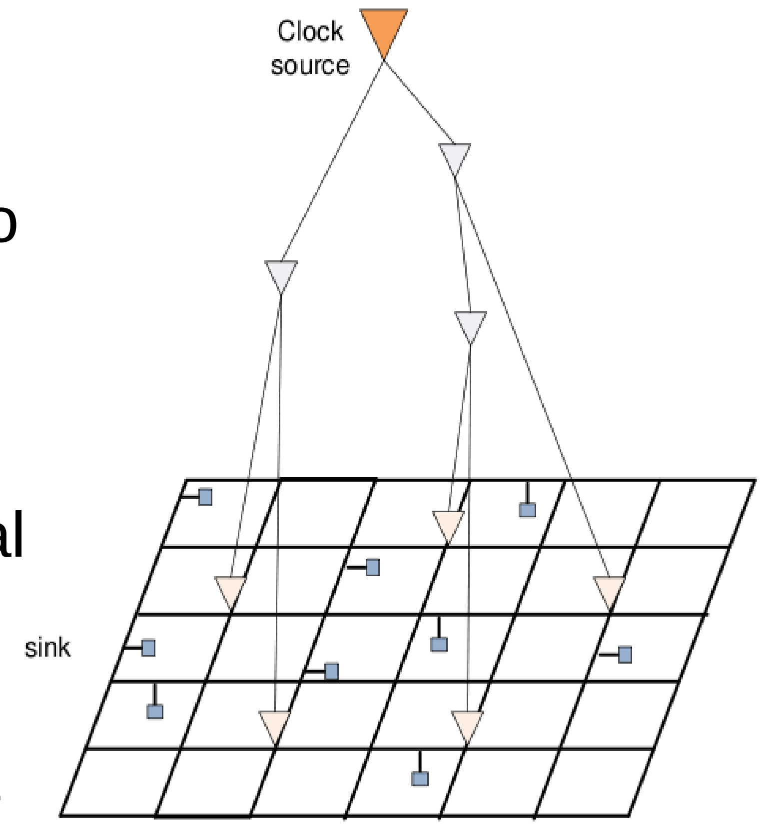


Clock Synthesis

- Clock Trees
  - Binary topology using nearest-neighbor clustering with a weighted combination of distance and insertion delay
  - Uses deferred merge embedding optimization
  - A minimal number of buffers are then inserted to preserve the slew constraints

Clock Synthesis

- Clock Grids
  - A top-level tree is used to drive a lower-level grid
  - Clock sinks are directly connected to the nearest wires
  - A quick buffer-insertion method is used to verify slew, and the grid is left over-buffered like many industrial designs
  - After being buffered wire removal is called to remove the wires that least affect the performance of the grid.



Setup

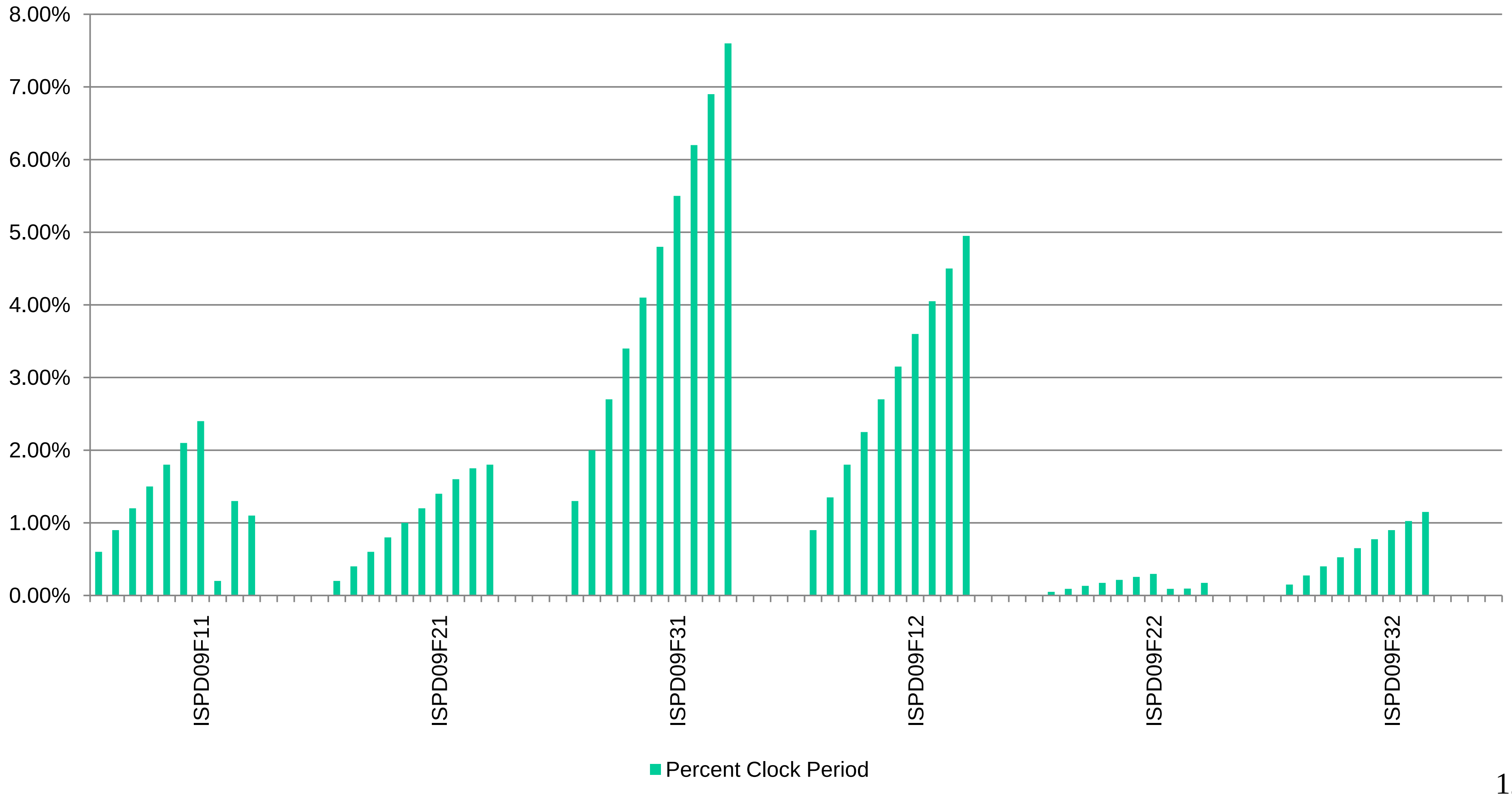
- We use the clock synthesis tool to generate a tree based upon the RC models

- At completion we switch the output to RLC or transmission line models without changing the physical structure

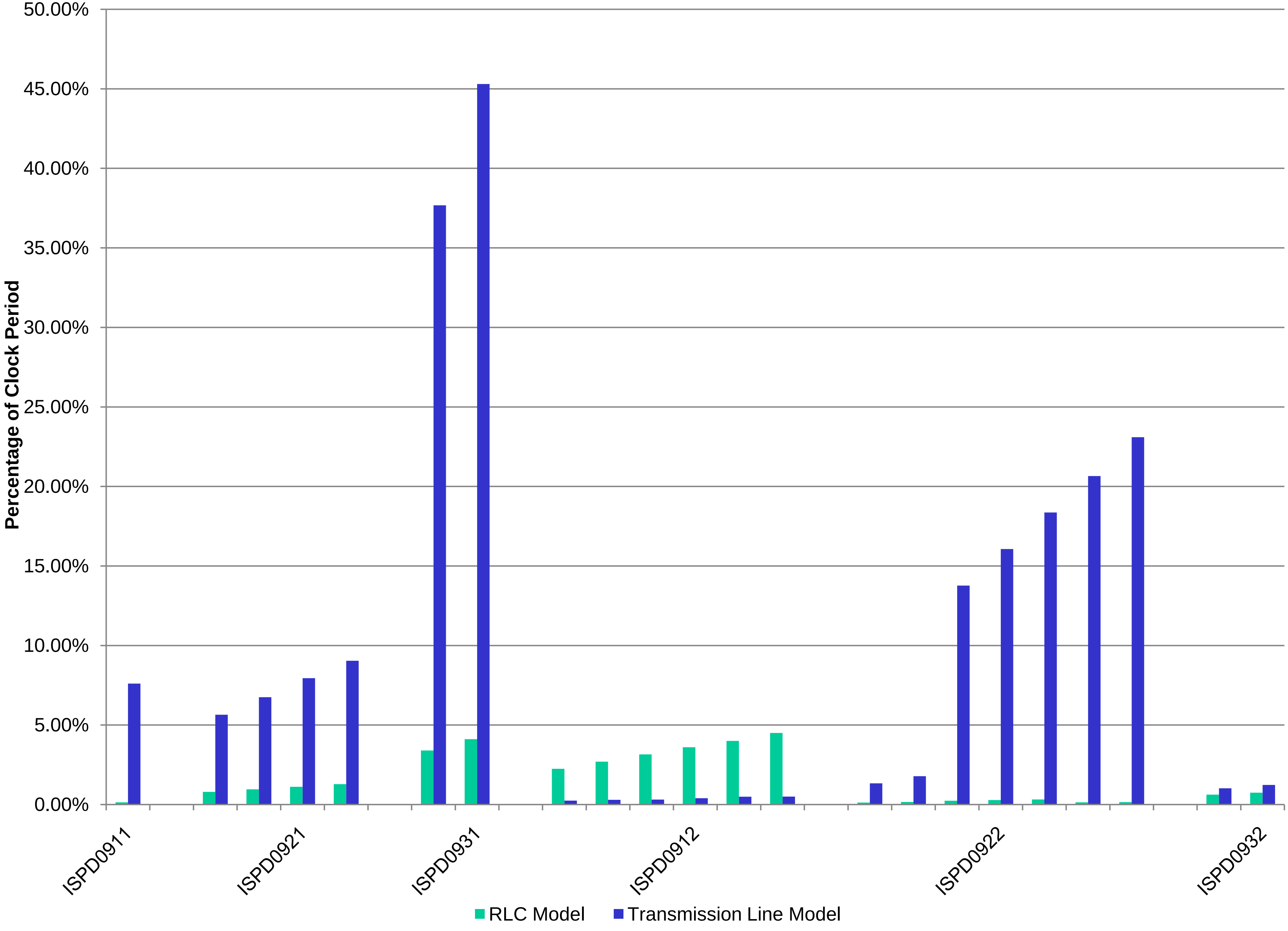
Measurement

- Two main types of measurement are taken
  - Skew
    - This is the primary metric of concern for this work
    - We measure worst skew amount all pairs of sinks at 50% of Vdd
    - $Skew = \max_{i \in Sinks}(t_i) - \min_{i \in Sinks}(t_i)$
  - Jitter
    - The only source of jitter considered is that of reflections
    - We measure periodic jitter over 10 cycles.
    - $J_i^2 = Var\left(t_{i,k+1} - t_{i,k}\right)$

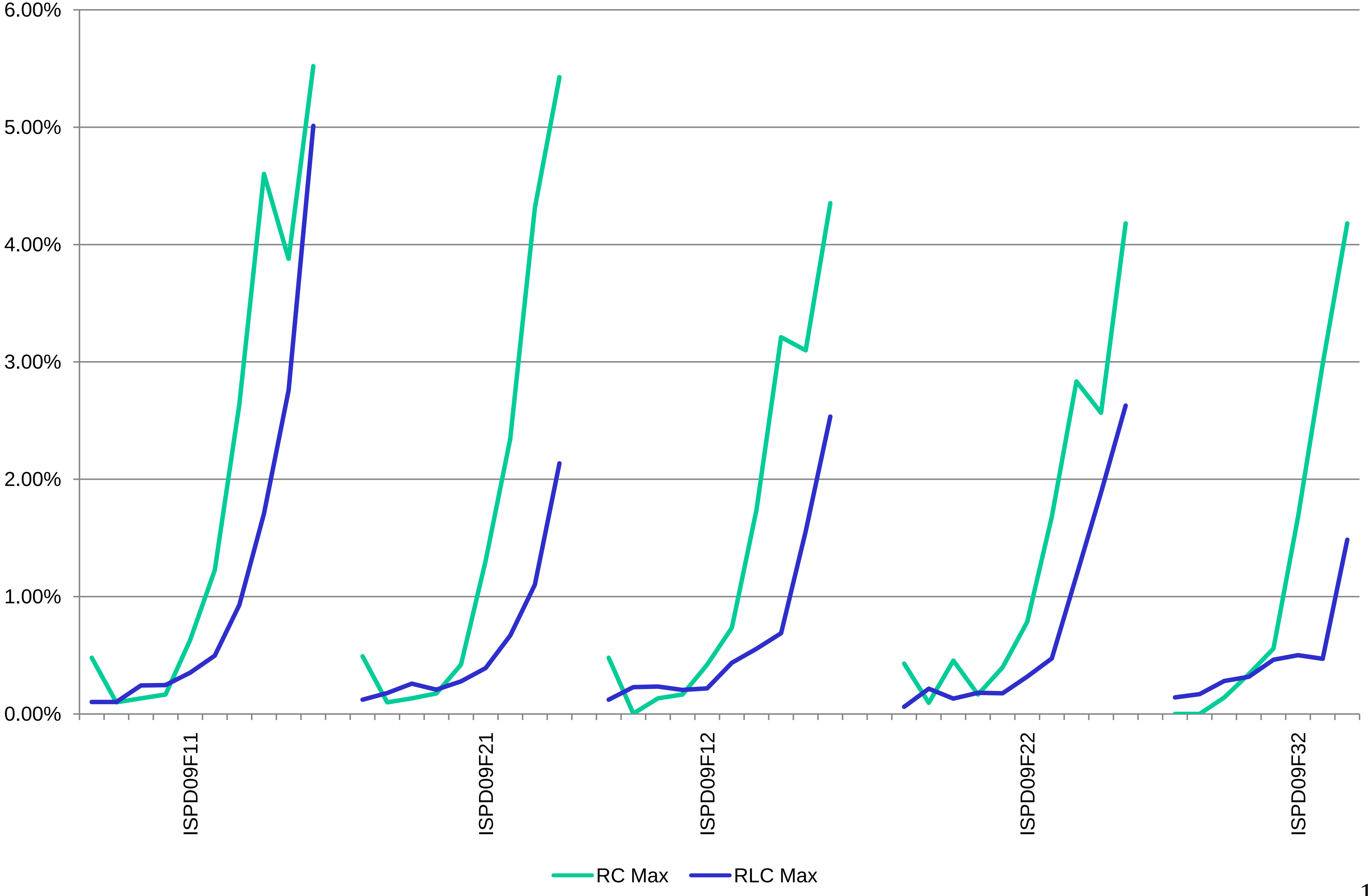
RLC Skew Results



Skew Results



Jitter Results



Summary

- Transmission Lines
  - Error as large as 45% of the clock period
- Jitter
  - As much as 5.5% of the clock period different from the RC model
- Slew
  - As slew was a primary constraint, this was kept uniform
- Grids
  - We note an error up to 80% of the clock period on grids

References

- [1] A. Kahng and C. Tsao, "Planar-DME: Improved Planar Zero-Skew Clock Routing With Minimum Pathlength Delay,,"" *Proc. European Design Automation Conference*, Citeseer, 1994, p. 440445.
- [2] G. Chen and E. Friedman, "An RLC interconnect model based on fourier analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, 2005, pp. 170-183.

Questions?