25th ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP)

www.SLIPonline.org

Co-located with ACM/IEEE Intl. Conf. on Computer-Aided Design Conference in San Francisco, CA, US, on November 2, 2023

Co-sponsored by ACM SIGDA and IEEE Computer Society TCVLSI

Accepted papers are published in an IEEE/ACM proceedings

GENERAL INFORMATION

The 2023 ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP) is the 25th edition of the Workshop. SLIP, co-located with ICCAD 2023, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology.

The technical goal of the workshop is to identify fundamental problems, and foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, DTCO/STCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, and new fabrics for the beyond-Moore era.

The submission process consists of two steps: abstract registration followed by regular technical paper submission in 6 to 8 pages, double-column, 9pt/10pt font in ACM proceedings format. To permit blind review, all papers must remove author information. Authors should submit papers electronically:
https://easychair.org/conferences/?conf=slip23
One author of accepted submission will present the work at the workshop. Accepted technical papers will be published in the ACM and IEEE digital libraries.

Organizing Committee:
Mustafa Badaroglu (Qualcomm), Shantanu Dutt (UIC), Pascal Vivet (CEA-LETI), Ismail Bustany (AMD), Seungwon Kim (Cadence), Rasit Topaloglu (IBM), Minsoo Kim (NVIDIA)

Steering Committee: Andrew Kahng (UC San Diego), Dirk Stroobandt (UGent), Baris Taskin (Drexel Univ), Mustafa Badaroglu (Qualcomm)

TECHNICAL TOPICS

Technical topics include but are not limited to:

- Learning and predictive models for interconnect at various IC and system design stages
- Roadmapping and pathfinding of on-chip interconnect, interconnect pipelining and 2.5D/3D chip-to-chip communication interfaces
- System-level design for FPGAs, NoCs reconfigurable systems, and domain-specific multi/many-core systems
- Design, analysis, and (co)optimization of power, clock distribution networks, and memory partitioning systems
- System-level interconnect reliability, aging, thermal, yield and cost issues
- Predictive models for power and performance of system-level interconnects
- Interconnects in bio-inspired systems, such as artificial neural networks and quantum architectures

SPECIAL SESSIONS

- Near/In memory compute and interconnect fabric for applications like generative AI and XR
- Chiplet interconnect fabrics (BOW, AIB, UCIe, etc) creating memory and compute coherency
- Backside metals for system interconnects such as power, IO, and clocking

IMPORTANT DATES

Abstract Registration: September 20, 2023
Paper Submission: September 24, 2023
Author Notification: October 8, 2023
Final Version Upload: October 15, 2023