

2022 ACM/IEEE System Level Interconnect Pathfinding Workshop
Technical Program
November 3, 2022

General Chair: Mustafa Badaroglu (Qualcomm)

Technical Program Chair: Shantanu Dutt (University of Illinois at Chicago)

Breaking the interconnect limits

Session Chair: Ismail Bustany (AMD)

Multi-die heterogeneous FPGAs: How balanced should netlist partitioning be? Raveena Raikar, Dirk Stroobandt (Ghent University)

Limiting interconnect heating in power-driven physical synthesis, Xiuyan Zhang, Shantanu Dutt (University of Illinois at Chicago)

2.5D/3D extension for high-performance computing

Session Chair: Pascal Vivet (CEA)

Opportunities of chip power integrity and performance improvement through wafer backside connection, Rongmei Chen, Giuliano Sisto, Odysseas Zografos, Dragomir Milojevic, Pieter Weckx, Geert Van Der Plas, Eric Beyne (IMEC) - invited

Compute-In-Memory and design of structured compute arrays

Session Chair: Shantanu Dutt (University of Illinois at Chicago)

An automated design methodology for computational SRAM dedicated to highly data-centric applications, Jean-Philippe Noel (CEA) – invited

A machine learning approach for accelerating SimPL-based global placement for FPGA's, Tianyi Yu², Nima Karimpour Darav¹, Ismail Bustany¹, Mehrdad Eslami Dehkordi¹ (¹AMD, ²University of Toronto)

Interconnect performance estimation techniques

Session Chair: Rasit Topaloglu (IBM)

Neural network model for detour net prediction
Jaehoon Ahn, Taewhan Kim (Seoul National University)

Machine-learning based delay prediction for FPGA technology mapping, Hailiang Hu², Fan Zhang¹, Ismail Bustany¹, Bing Tian¹, Jiang Hu² (¹AMD, ²Texas A&M University)

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