

FINAL PROGRAM

SLIP 2014 Technical Program

June 1st, 2014

Co-located with DAC in San Francisco

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Breakfast (8:00am-8:30am)

Opening Remarks (8:30am-8:40am)

Session I: 3D Integration (Chair: Akhilesh Kumar, Intel)

- **8:40am – 9:10am:** “Compact Models and Model Standard for 2.5D and 3D Integration”, Qiaosha Zou and Yuan Xie, Penn State Univ. **(INVITED)**
- **9:10am – 9:40am:** “Computing in 3D”, Paul Franzon, NC State Univ. **(INVITED)**
- **9:40am – 10:10am:** “Monolithic 3D Integration of Logic and Memory”, H.-Y. Chen, M. Shulaker, S. Yu, H. Wei, B. Gao, J. Kang, S. Mitra, and H.-S. P. Wong, Stanford Univ. **(INVITED)**
- **10:10am – 10:25am:** Post-session Review Panel (Expert Panelist: Akhilesh Kumar, Intel)

Break (10:25am – 10:45am)

Session II: Power and Clock Delivery (Cliff Sze, IBM)

- **10:45am – 11:05am:** “Power Network On-Chip for Scalable Power Delivery”, Inna Vaisband and Eby Friedman, Univ. of Rochester
- **11:05am – 11:25am:** “Worst-Case Noise Area Prediction of On-Chip Power Distribution Network”, Xiang Zhang, Jingwei Lu, Yang Liu and Chung-Kuan Cheng, Xidian Univ. & UC San Diego
- **11:25am – 11:45am:** “PACMAN: Driving Nonuniform Clock Grid Loads for low-skew robust clock network”, N. Zhou, P. Restle, J. Palumbo, J. Kozhaya, H. Qian, C. Sze, Z. Li and C. Alpert, IBM Research
- **11:45am – 12:00pm:** Post-session Review Panel (Expert Panelist: Cliff Sze, IBM)

Lunch (12:00pm – 1:00pm)

Session III: Routing (Chair: Chung-Kuan Cheng, UC San Diego)

- **1:00pm – 1:30pm:** “Manufacturable and Reliable Interconnect in Extreme Scaling”, David Pan, UT Austin **(INVITED)**
- **1:30pm – 1:50pm:** “UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm”, Tsung-Wei Huang, Pei-Ci Wu and Martin D. F. Wong, UIUC
- **1:50pm – 2:10pm:** “Range-based Dynamic Routing of Hierarchical On Chip Network Traffic”, Julian Kemmerer and Baris Taskin, Drexel Univ.
- **2:10pm – 2:30pm:** “Methodology for Electromigration Signoff in the Presence of Adaptive Voltage Scaling”, Wei-Ting Chan, Andrew B. Kahng and Siddhartha Nath, UC San Diego
- **2:30pm – 2:45pm:** Post-session Review Panel (Expert Panelist: Chung-Kuan Cheng, UC San Diego)

Break (2:45pm – 3:00pm)

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Poster Session and Networking

3:00pm – 3:30pm

- “Site Functions for 3D ICs Considering Impacts of TSVs”, Masoud Zabihi, Farzad Radfar and Reza Sarvari, Sharif Univ. of Technology
- “Toward Assessment of True 3D Design Benefits over 2D Implementation”, Tuck-Boon Chan, Andrew B. Kahng, Ilgweon Kang, Hyein Lee and Jiajia Li, UC San Diego

Invited Talk: On AMBA Interconnect (Rob Aitken, ARM)

3:30pm – 4:00pm

Panel: Emerging Technologies and Networks-on-Chip (NoC) Design (Chair: Umit Ogras, ASU)

4:00pm – 5:00pm

Panelists:

- Prof. Yuan Xie, The Pennsylvania State Univ., “NoCs with 3D IC technology”
- Prof. Partha Pratim Pande, Washington State Univ., “NoCs with wireless communication technology”
- Prof. Wim Boaerts, Ghent Univ. – IMEC, “NoCs with Optical Communication Technology”
- Dr. Akhilesh Kumar, Intel Corporation, “High bandwidth industrial NoC design”

Dinner (6:30pm)

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IBM, USA

Technical Program Chair

Sung Kyu Lim
Georgia Institute of Technology, USA

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Baris Taskin
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