## SLIP 2011 Technical Program

## June 5th, 2011. Co-located with DAC at San Diego Convention Center

**Breakfast** **8:00am - 8:30am**

**Welcome Message + Keynote Speech** **8:30am - 9:30am**
Riko Radojcic, QualComm Inc.
**Title: Design Eco-System for 3D Integration – an IFM Perspective**

**Coffee Break** **9:30am - 9:45am**

**Session I: TSV Scaling and 3D FPGA** **9:45am - 10:35am**
**Session Chair:** Sherief Reda, Brown University, USA

*Impact of Nano-scale Through-Silicon Vias on the Quality of Today and Future 3D IC Designs*
Dae Hyun Kim, Suyoun Kim and Sung Kyu Lim, Georgia Institute of Technology
9:45am-10:05am

*Architecture and Performance Evaluation of 3D CMOS-NEM FPGA*
Chen Dong*, Chen Chen+, Subhasish Mitra+, and Deming Chen*, * University of Illinois at Urbana Champaign; + Stanford University
10:05am-10:25am

**Discussion Panel –** Robert Patti (Tezzaron), Riko Radojcic (QualComm), Sherief Reda (Brown University)
10:25am-10:35pm

**Coffee Break** **10:35am - 10:50am**

**Session II: Multicore and Embedded SoC Design** **10:50am - 12:30pm**
**Session Chair:** Chung-Kuan Cheng, University of California at San Diego, USA

(*Invited Talk*)
Luca Benini, Università di Bologna, Italy
**Title: Many-core Interconnection Networks Trends: Fast, Vertical, Asynchronous**
10:50am-11:20am

*Reducing Energy and Increasing Performance with Traffic Optimization in Many-core Systems*
George Bezerra, Stephanie Forrest and Payman Zarkesh-Ha, Univeristy of New Mexico
11:20am-11:40am

*System Interconnect Design Exploration for Embedded MPSoCs*
Chen-Ling Chou*, Radu Marculescu+, Umit Ogras#, Satrajit Chatterjee#, Michael Kishinevsky# and Dmitrii Loukianov#, * General Electric Inc.; + Carnegie Mellon University; # Intel Inc.

11:40am-12:00am

*Mobile System Considerations for SDRAM Interface Trends (short)*
Andrew Kahng* and Vaishnav Srinivas+, * University of California at San Diego; + QualComm Inc.
12:00am-12:15pm

**Discussion Panel –** Luca Benini (Università di Bologna), C. K. Cheng (UCSD), Colin Dente (Akya Limited)
12:15pm-12:30pm

**Lunch 12:30pm - 1:30pm**

**Session III: Advanced Techniques on Routing 1:30pm - 2:35pm**
**Session Chair:** Hui-Ru Jiang, National Chiao Tung University, Taiwan

*A SAT-Based Routing Algorithm for Cross-Referencing Biochips*
Ping-Hung Yuh*, Cliff Chiung-Yu Lin+, Tsung-Wei Huang#, Tsung-Yi Ho#, Chia-Ling Yang& and Yao-Wen Chang&, * TSMC; + Stanford University; # National Cheng Kung University; & National Taiwan University
1:30pm-1:50pm

*Interface Optimization for Improved Routability in Chip-Package-Board Co-Design (short)*
Tilo Meister*, Jens Lienig* and Gisbert Thomke+, * Dresden University of Technology; + IBM Deutschland Research and Development
1:50pm-2:05pm

*Stability and Scalability in Global Routing (short)*
Sung Kyu Han, Kwangok Jeong, Andrew Kahng and Jingwei Lu, University of California San Diego
2:05pm-2:20pm

**Discussion Panel –** Chuck Alpert (IBM), Laleh Behjat (University of Calgary), Hui-Ru Jiang (National Chiao Tung University)
2:20pm-2:35pm

**Coffee Break + Poster Session 2:35pm - 3:00pm**

*Performance and Power Analysis of Through Silicon Vias based 3D ICs Integration*
Hung Viet Nguyen, Myunghwan Ryu, and Youngmin Kim, UNIST, Korea

*Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 2D Wireless NoC*
Ankit More and Baris Taskin, Drexel University

*Wirelength and Congestion Estimation for Routability-Driven Placement*
Yangyang Li*, Logan Rakai*, Bill Swartz+, and Laleh Behjat*, * University of Calgary, Canada; + InternetCad.com, Inc.

**Panel: TSV-based 3D ICs: Why Does It Take So Long? 3:00pm - 4:00pm**
Moderator: Sung Kyu Lim, Georgia Institute of Technology, USA
**Panelists: Paul Franzon (North Carolina State University), Sam Gu (QualComm), Dragomir Milojevic (IMEC), Robert Patti (Tezzaron Semiconductor)**

**Coffee Break + Poster Session 4:00pm - 4:15pm**

**Session IV: Power Network Resource Estimation and Design 4:15pm - 5:30pm**
**Session Chair:** Baris Taskin, Drexel University, USA

*(Invited Talk)*
Nagaraj NS, TI
**Title: Performance and Power Optimization in Sub-20nm Era**
4:15pm-4:45pm

*Toward PDN Resource Estimation: A Law of Power Density*
Kwangok Jeong and Andrew Kahng, University of California, San Diego
4:45pm-5:05pm

*Distributed Power Network Co-Design with On-Chip Power Supplies and Decoupling Capacitors (short)*
Selcuk Kose and Eby G. Friedman, University of Rochester
5:05pm-5:20pm

**Discussion Panel –** Tsung-Yi Ho (National Cheng Kung University), Youngmin Kim (UNIST), Baris Taskin (Drexel University)
5:20pm-5:30pm

**Banquet Dinner + Banquet Plenary Talk 6:30pm - 8:30pm**

Chuck Alpert, IBM
**Title: Devil Is in the Detailed Router: Congestion Hotspot Prediction**