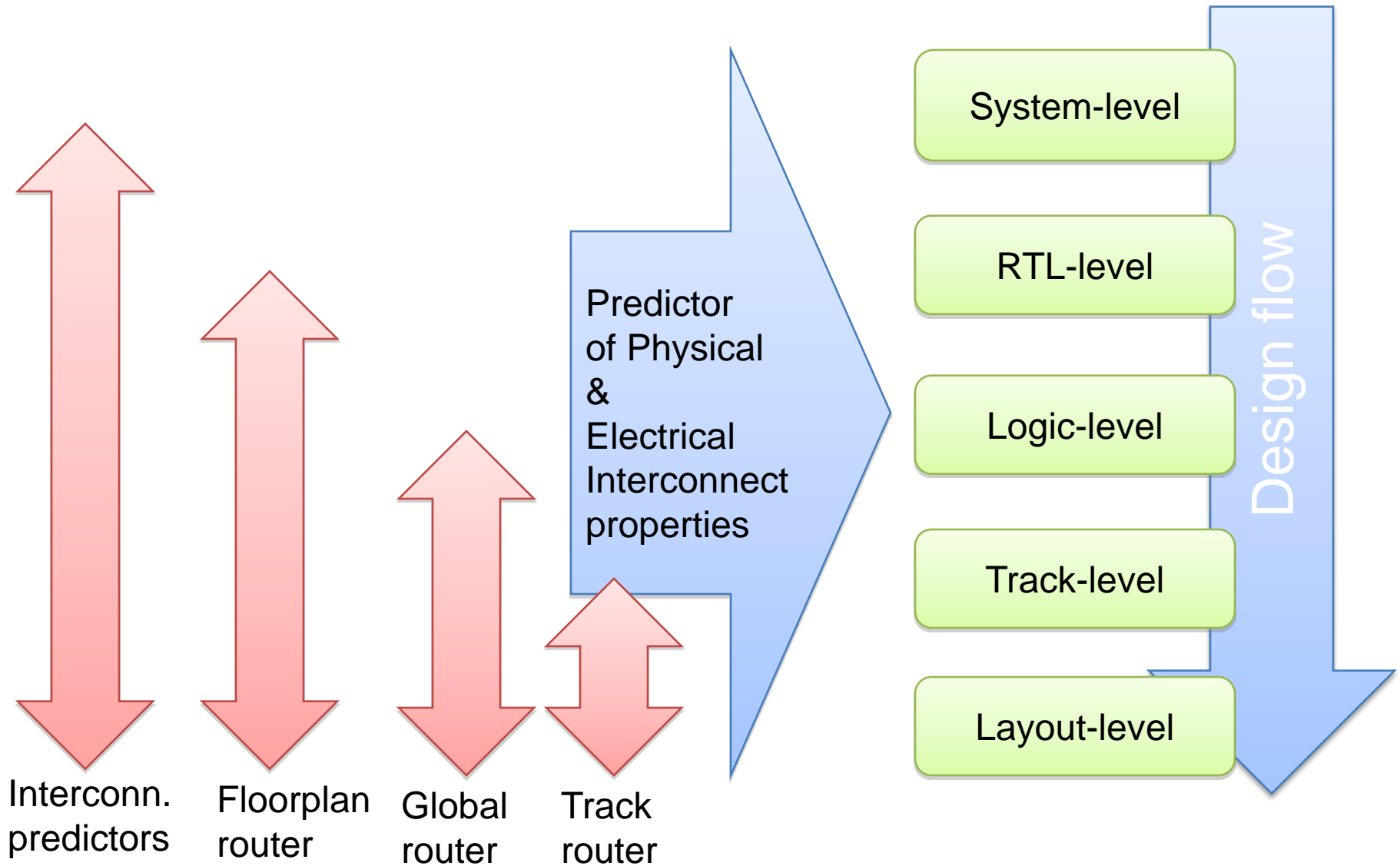


SLIP: Past, Present and Future

Patrick Groeneveld
Chief Technologist, Magma Design Automation

Fastest Path to Silicon

Interconnect Prediction: big picture

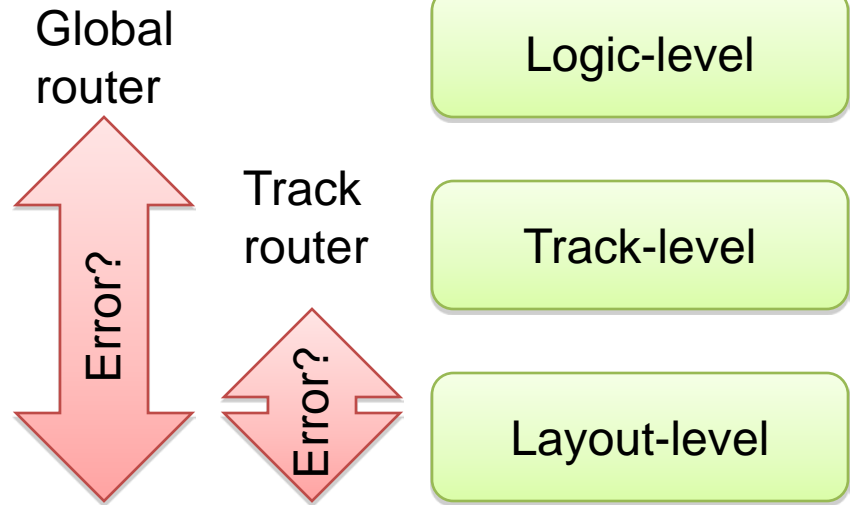


Interconnect Prediction error: Hard data

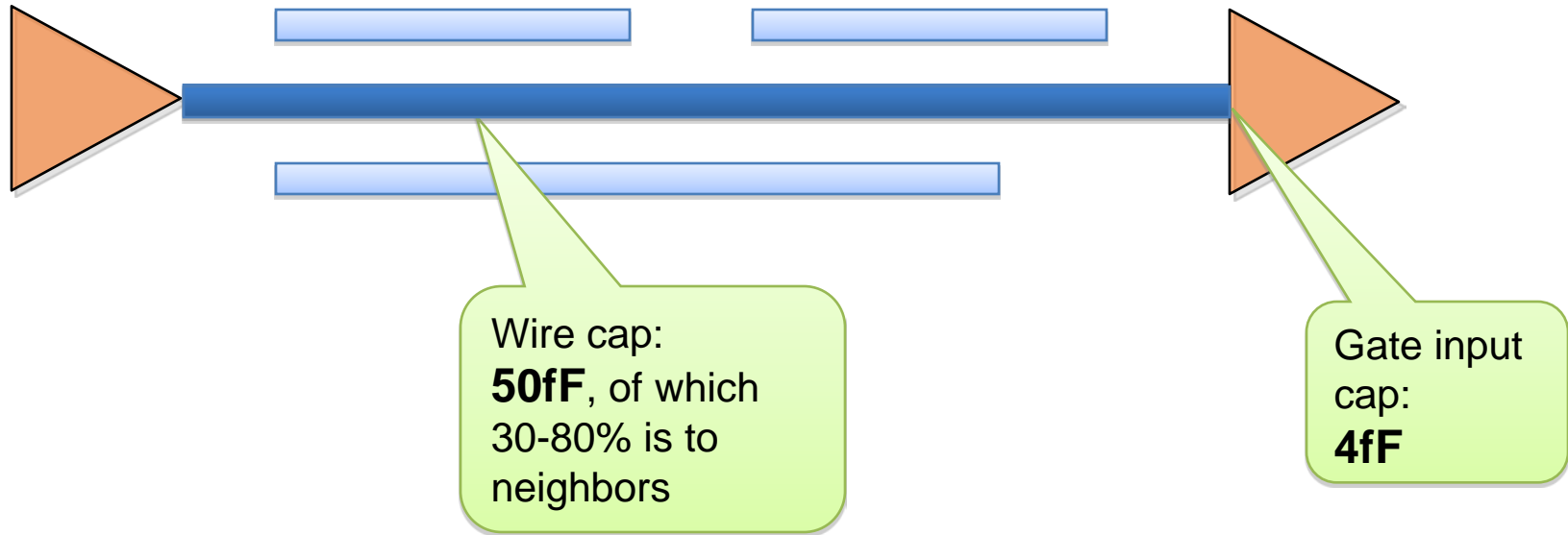
7 real designs,
300K-2.9M nets
45nm & 32nm
technologies

NET DELAY				NET Capacitance			
Global	Track	Global	Track	Global	Track	Global	Track
Standard Deviation		worse than 5% off		error in average		Standard Deviation	
77.3%	34.5%	96.8%	89.6%	-9.0%	2.8%	39.7%	20.0%
83.1%	43.0%	91.4%	91.6%	2.3%	-0.4%	10.4%	8.8%
60.1%	40.7%	99.6%	93.6%	1.20%	0.80%	11.20%	10.20%
51.3%	37.0%	97.5%	80.2%	6.00%	2.90%	8.50%	4.30%
123.6%	73.5%	97.9%	87.8%	0.30%	0.90%	9.50%	7.80%
56.0%	32.8%	96.1%	83.2%	6.90%	2.80%	9.80%	5.40%
163.0%	29.4%	99.0%	87.3%	-4.30%	0.30%	7.60%	5.10%
87.8%	41.6%	96.9%	87.6%	0.5%	1.4%	13.8%	8.8%
87.8%	41.6%	96.9%	88.5%	4.6%	1.4%	13.8%	8.8%

Why is the
Global-level
Interconnect
delay prediction
so *terribly* off?

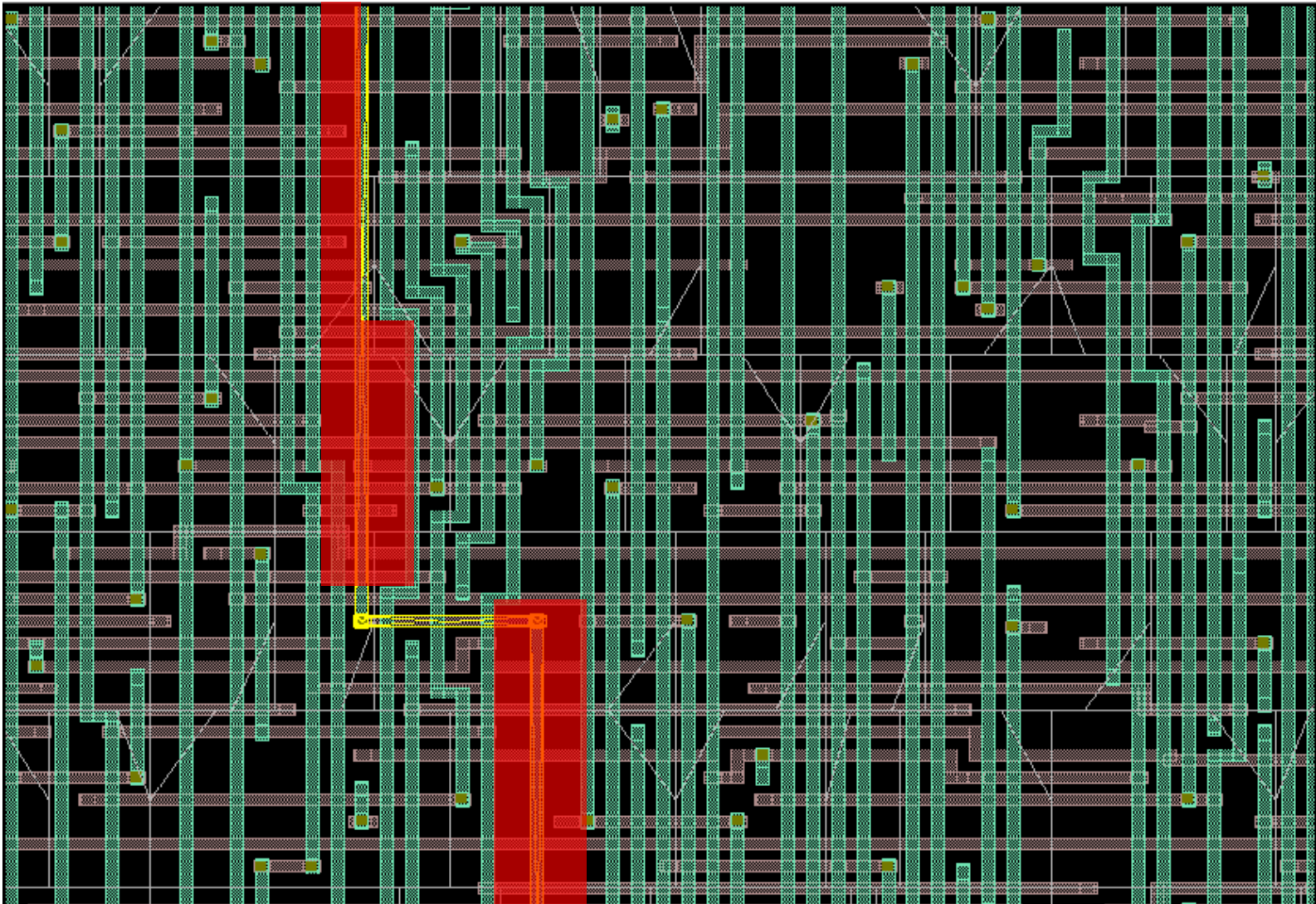


Interconnect planning: area vs. predictability



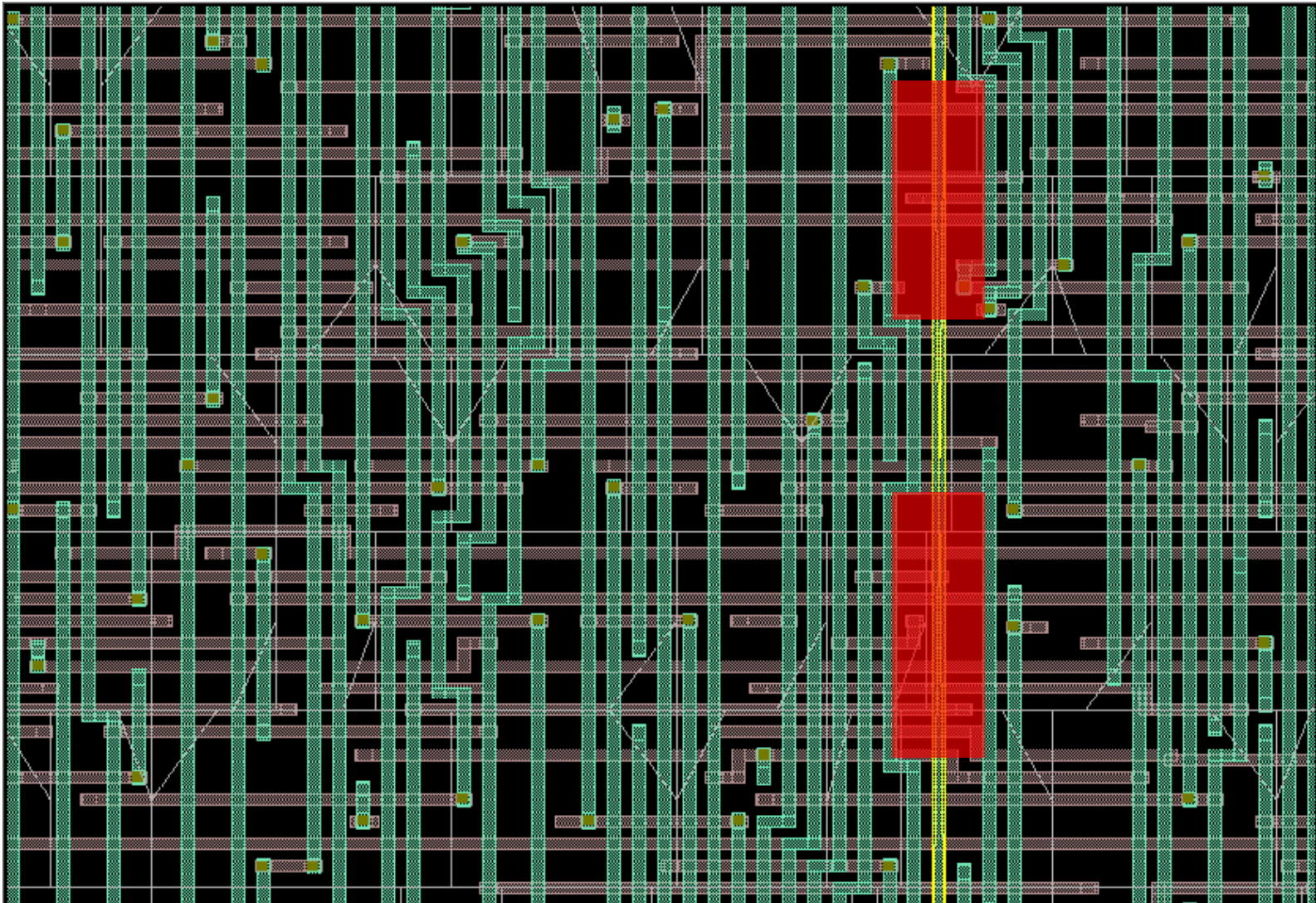
- Delay depends on:
 - Drive strength, wire resistance (predictable)
 - Capacitive load of wires and pins (predictable)
 - Slew and proximity of neighbors (yikes!)

Pushing neighbors away



Fastest Path to Silicon

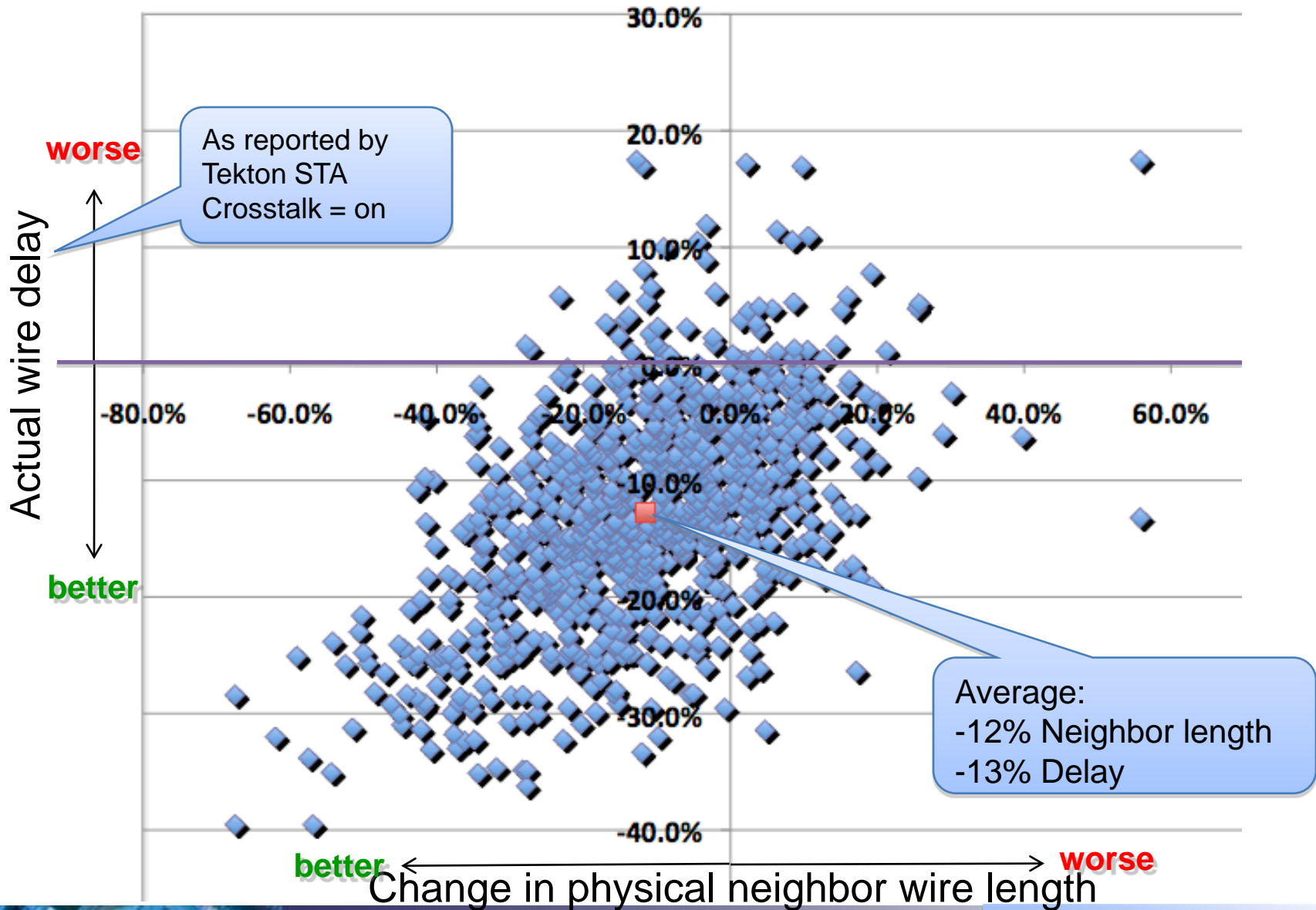




Fastest Path to Silicon



Effect of this physical ECO on timing



My take on SLIP

- Non-physical (a-priori) interconnect estimation is simply not so relevant
 - Interconnect prediction needs real placement/floorplan
- Physical Interconnect estimation is extremely relevant to feed into synthesis tools
- Need detailed correlation studies
 - Its unlikely that elegant models work.
- More links with physical synthesis algorithms
 - Floor planning, placement logic optimization

SLIP 2000, 2010, 2020

Rent paper frequency at SLIP during the past decade



Interconnect Prediction: papers I'd like to see

- **“Finding the optimal sweet spot between interconnect supply and timing constraints”**, Proc. Interconnect workshop, Hawaii, 2012
- **“A fast and efficient interconnect performance estimator for ESL level floorplanning”** Proc Interconnect workshop, 2013
- **“A New wire performance model for global placement”**, Proc Interconnect workshop 2011
- **“Measurement techniques and interconnect estimation”**
- **“Why interconnect prediction doesn't work”**
- **“Fast, Accurate Routing Delay Estimation”**

SLIP2000
SLIP2000
SLIP2010