3-2-1 Contact: An Experimental Approach to the Analysis of Contacts in 45 nm and Below

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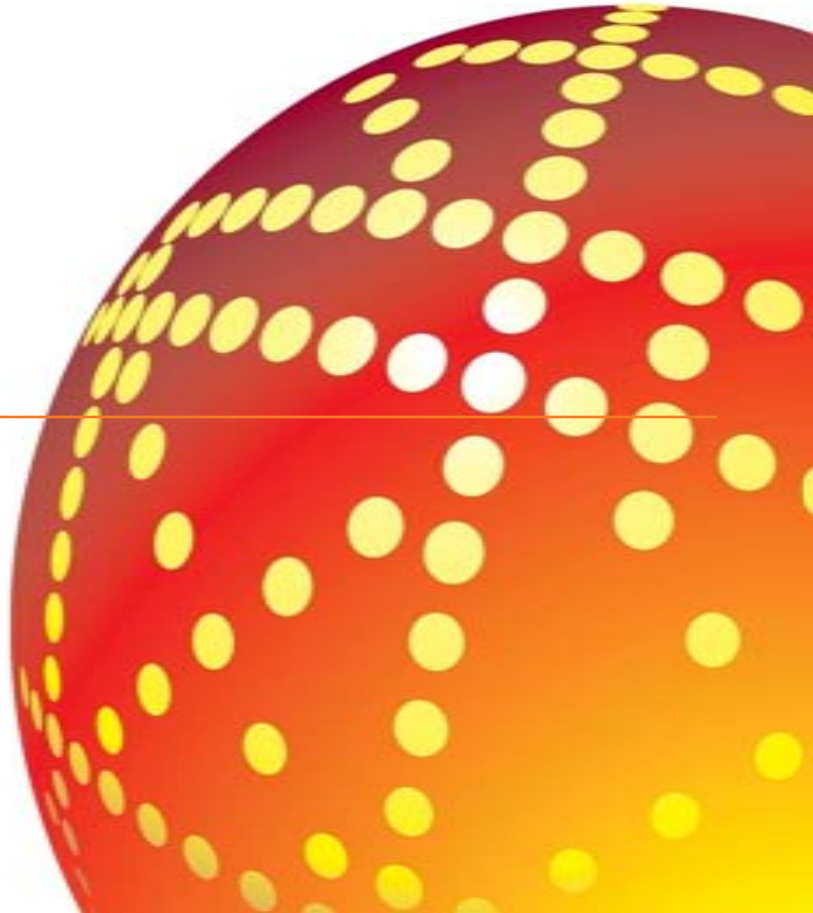
GLOBALFOUNDRIES



Outline

- Introduction and Motivation
- Impact of Contact Resistance
- Test Structures for Contact Resistance
- Contact-Level Routing
- Conclusions

Increase of Contact Resistance

- In new technologies, contact resistance is increasing due to
  - smaller diameter
  - surface scattering
  - taller contacts
- Contact resistance targets over two technology generations are given below:

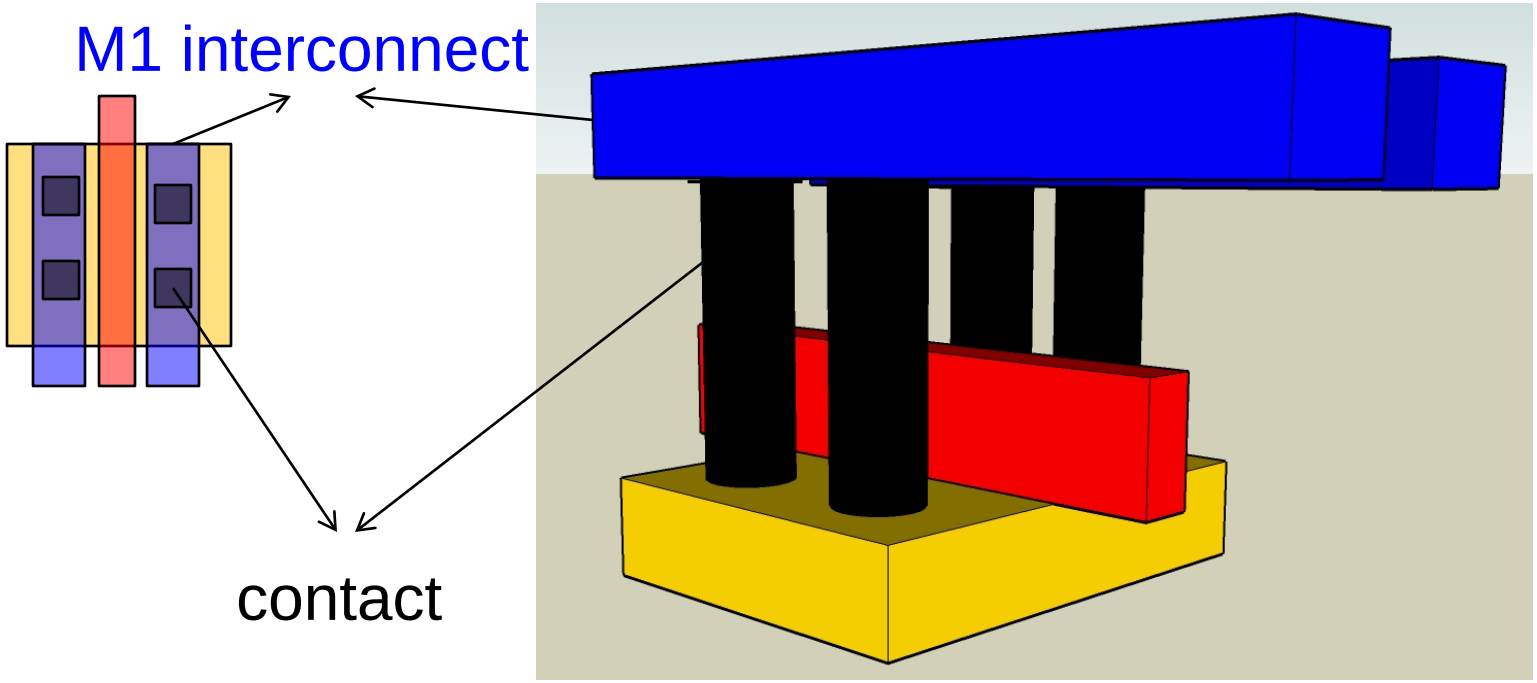
Technology	Min	Mean	Max
65 nm	10 Ω	20 Ω	50 Ω
45 nm	20 Ω	40 Ω	100 Ω

- Notice the increase in mean and standard deviation

Contact Resistance in Device Characterization

MOSFET layout

Physical view



- Contacts provide connectivity between transistor drain and source to interconnects
- When measuring devices, even for wafer-level measurements on M1, contact resistance is involved

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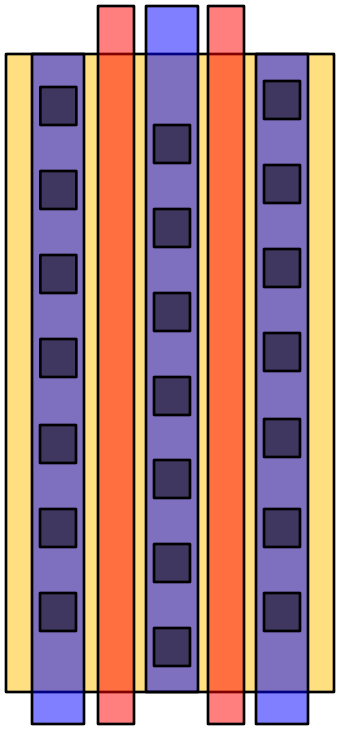
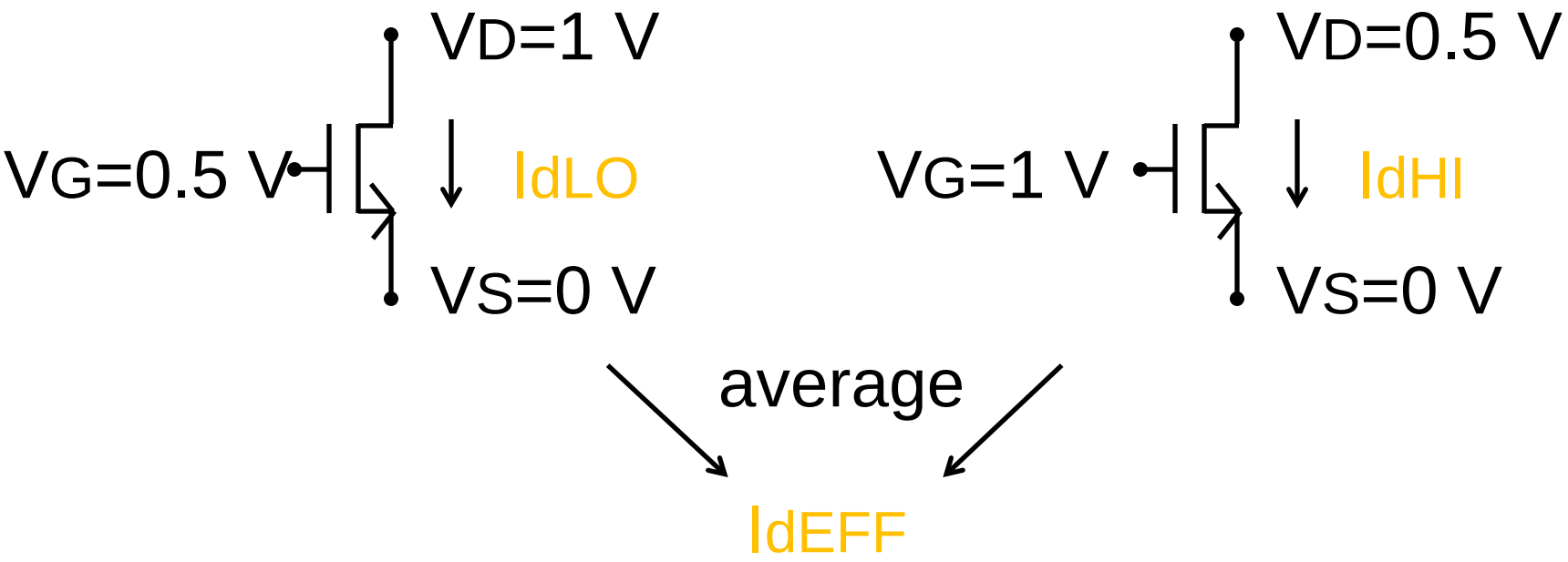
Resistance-Capacitance Trade-Off



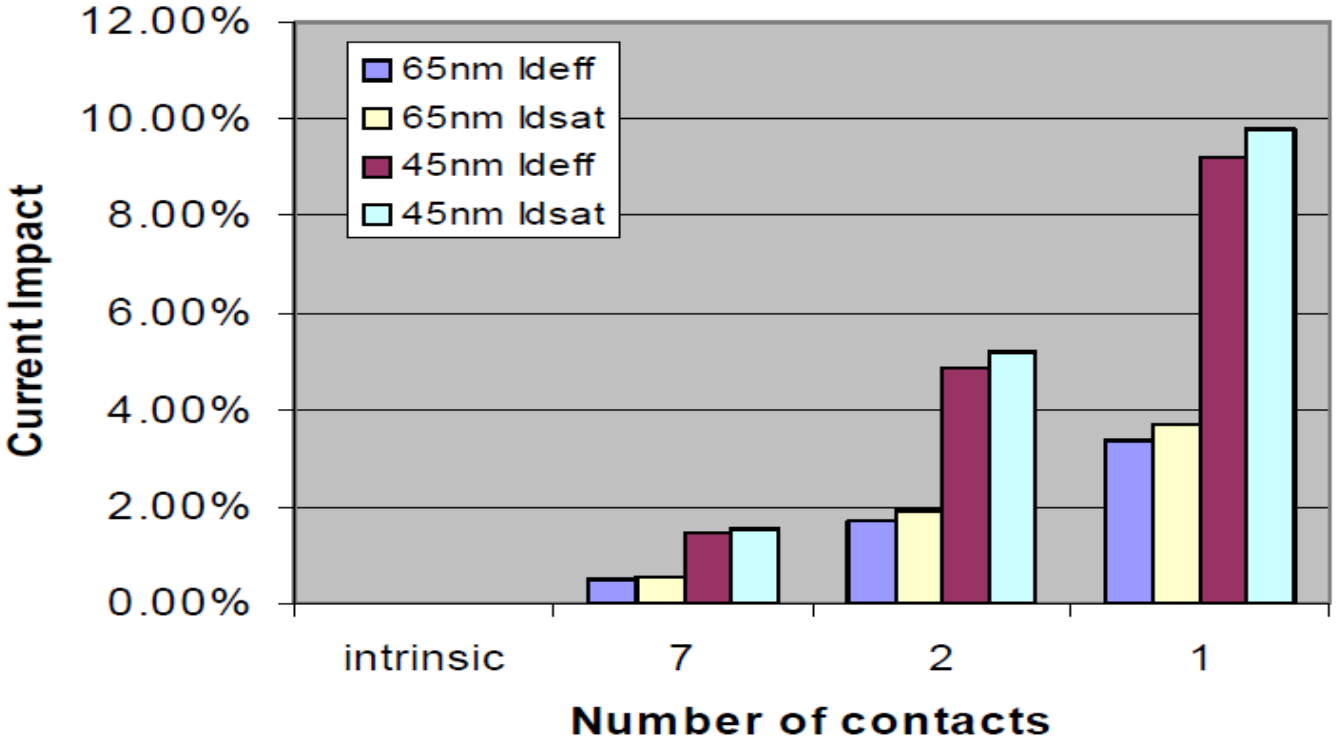
- Higher number of contacts increase gate to contact coupling capacitance
  - Results in slower circuits
- Lower number of contacts increases resistance to device terminals
  - Smaller drain current
  - May result in design rule violations
  - May result in extraction inaccuracies

Drain Current Definitions in Experiments

- Wafer electrical tests need to be fast as hundreds of devices are measured
- Instead of full current-voltage sweep, representative electrical parameters are frequently used



Contact Count Impact on Drain Current



- Data is silicon-influenced and model-based
- Maximal impact increases from 3.3% in 65 nm to 9.21% in 45 nm

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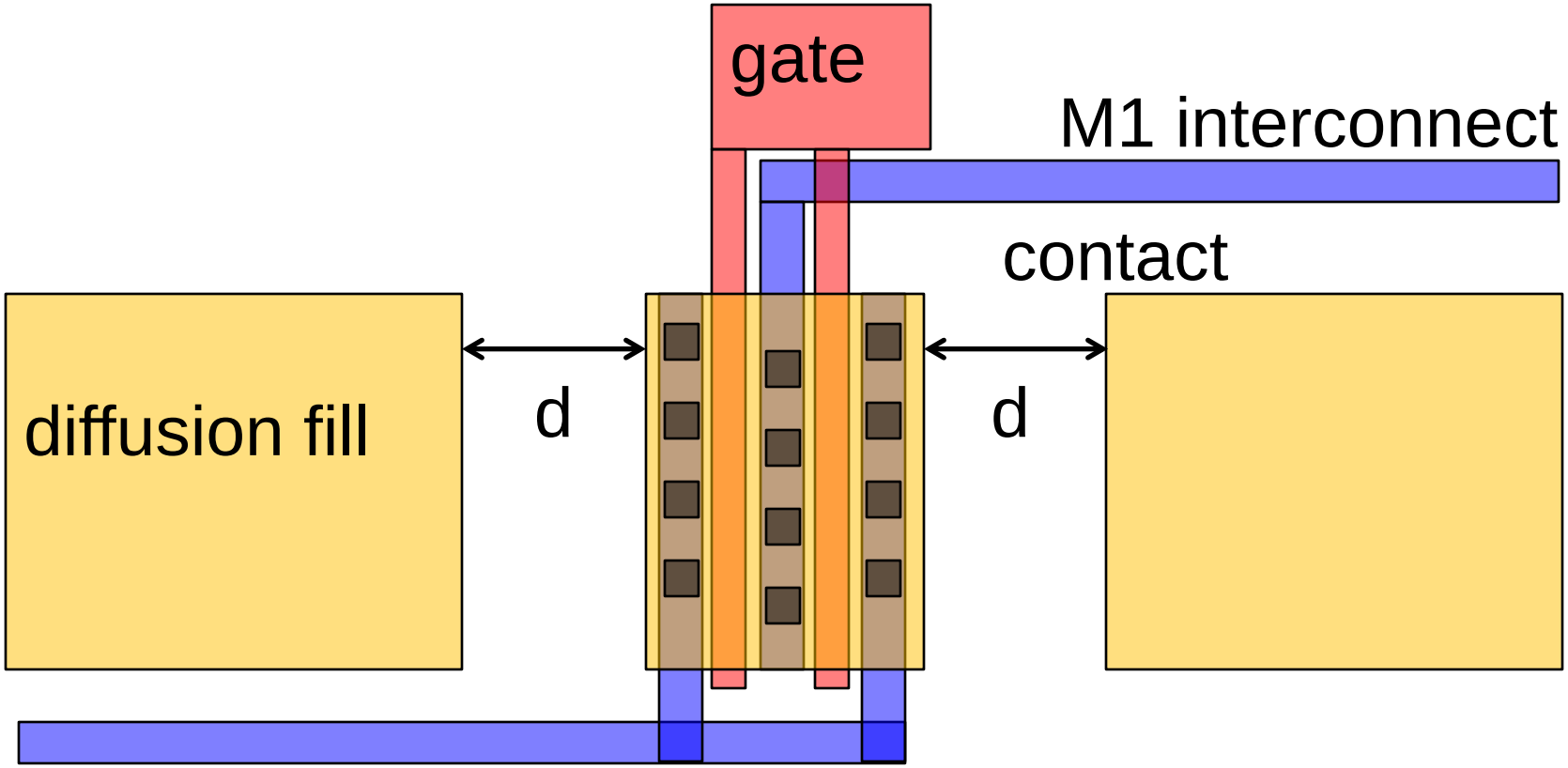
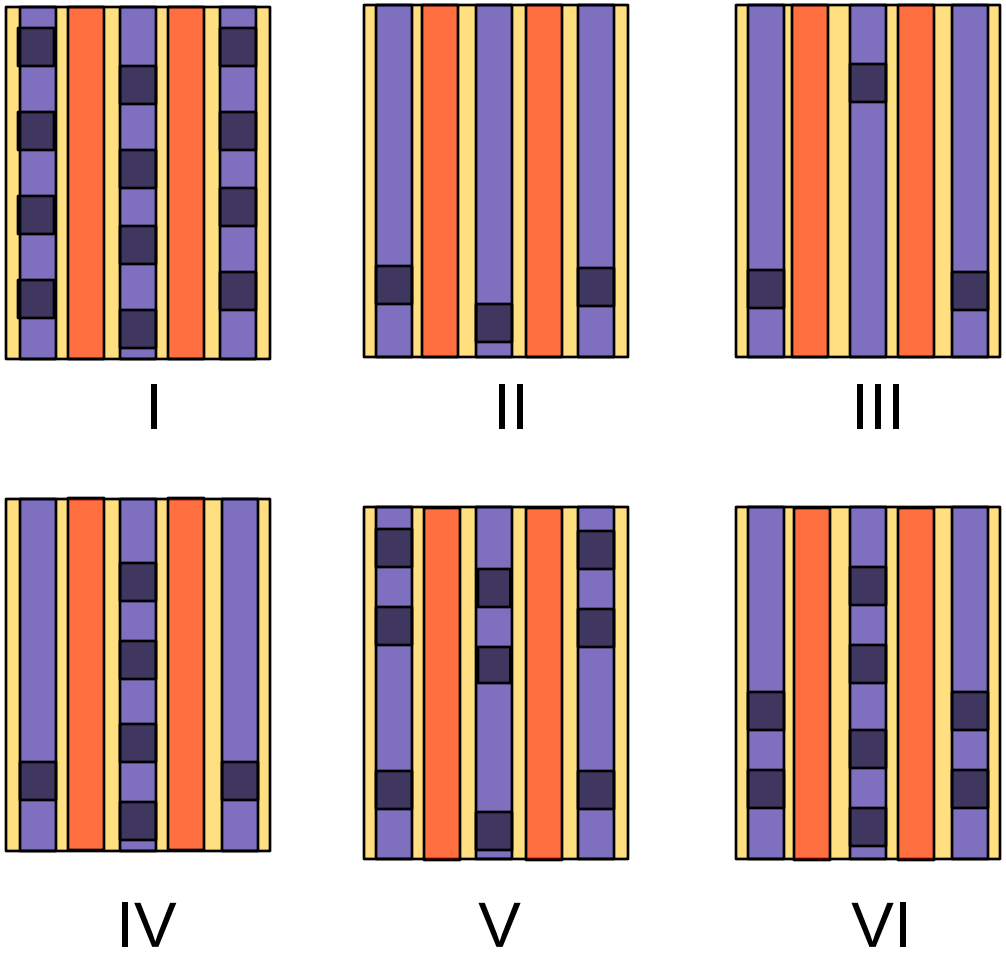
Test Structure Template

- We use diffusion fills to control STI width stress [1]
- Contact number is adjustable



[1] R.O. Topaloglu, Proceedings of IEEE CICC, 2007

Test Structures and Silicon Results

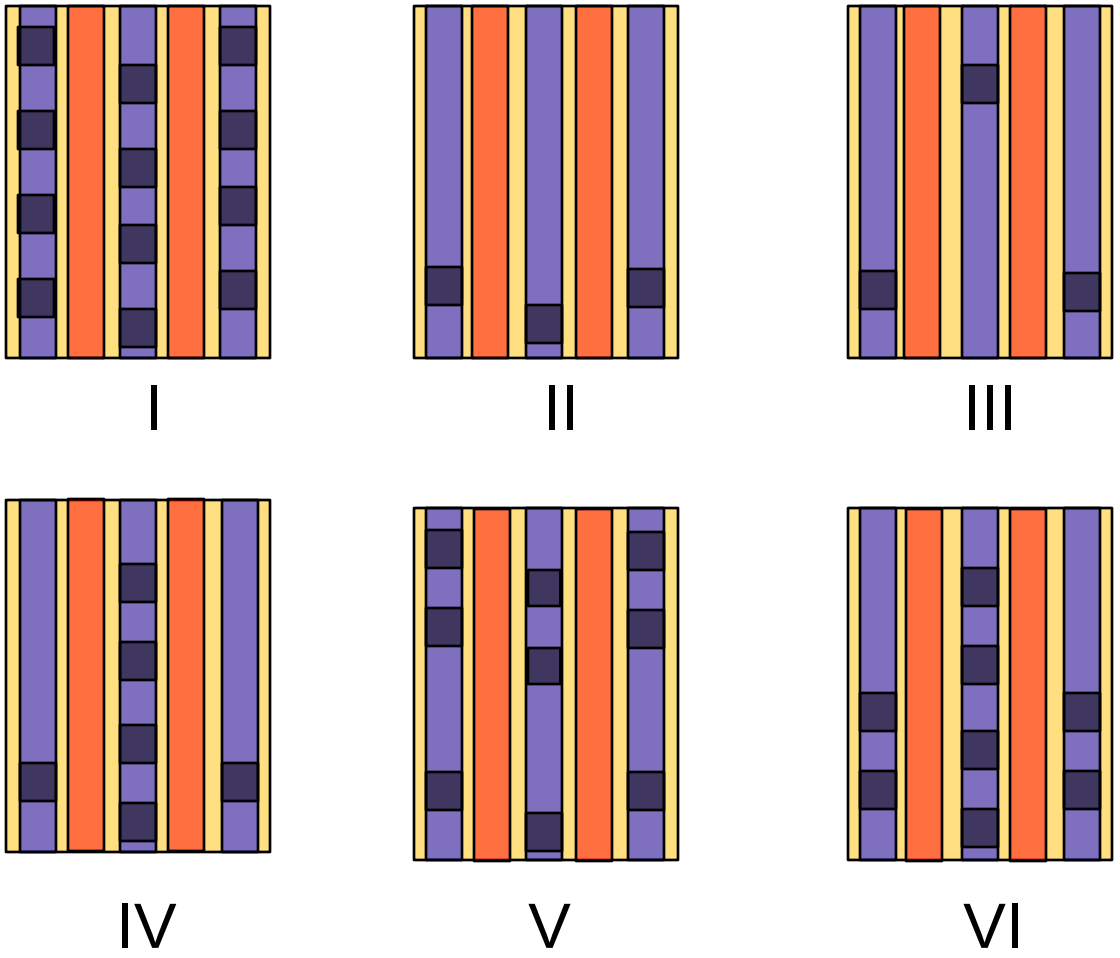


	Gate	Contact	M1	V1
Height	80	240	120	120
Width	40	40	60	55

No	Ideff (μA/μm)	Impact
I	499.09	0.00%
II	416.69	16.51%
III	413.73	17.10%
IV	442.03	11.43%
V	476.17	4.59%
VI	466.92	6.44%

- Different contact configurations mimic various design styles in custom layouts and standard cells

Test Structures and Capacitance Results



No	Capacitance (fF)
I	8.28E-2
II	1.32E-2
III	1.35E-2
IV	4.80E-2
V	3.79E-2
VI	5.38E-2

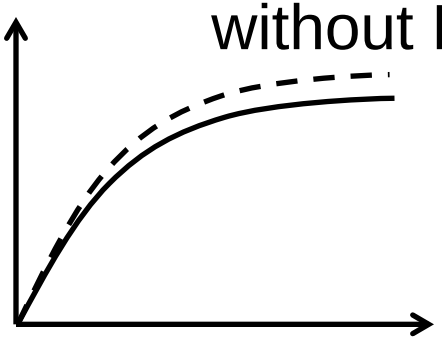
- More contacts result in increased coupling

SPICE Modeling and Circuit Implications

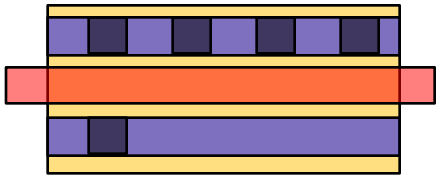
- RC extractors are suboptimal when transistors are not fully contacted
  - Double counting is possible for contact resistance
  - May result in coupling capacitance inaccuracy

device model with R impact ——

without R - - -



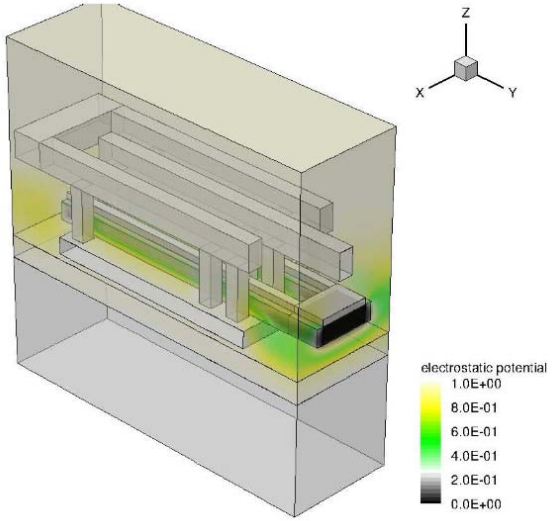
Some RC extractors assume devices are fully contacted or are inaccurate

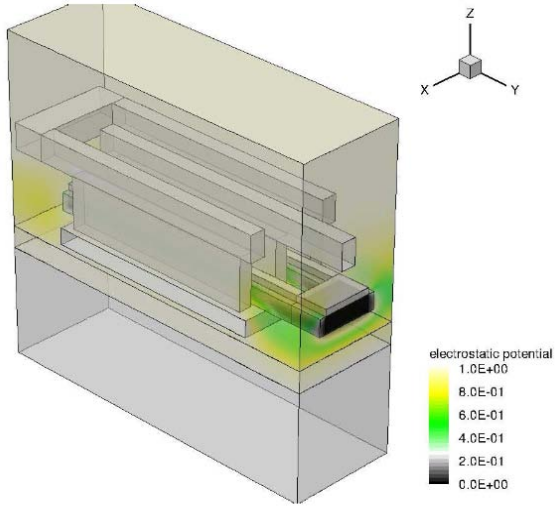


- We generate models which are not contaminated by resistance; we also work with EDA vendors for more accurate capacitance extraction

How to Reduce Contact Resistance?

- Option 1: Use copper instead of tungsten
- Option 2: Merge contacts, i.e., use contact bars





- Capacitive coupling increases to 10.20E-2fF
  →only 1.23x as compared to fully contacted
  →up to 2x resistance improvement

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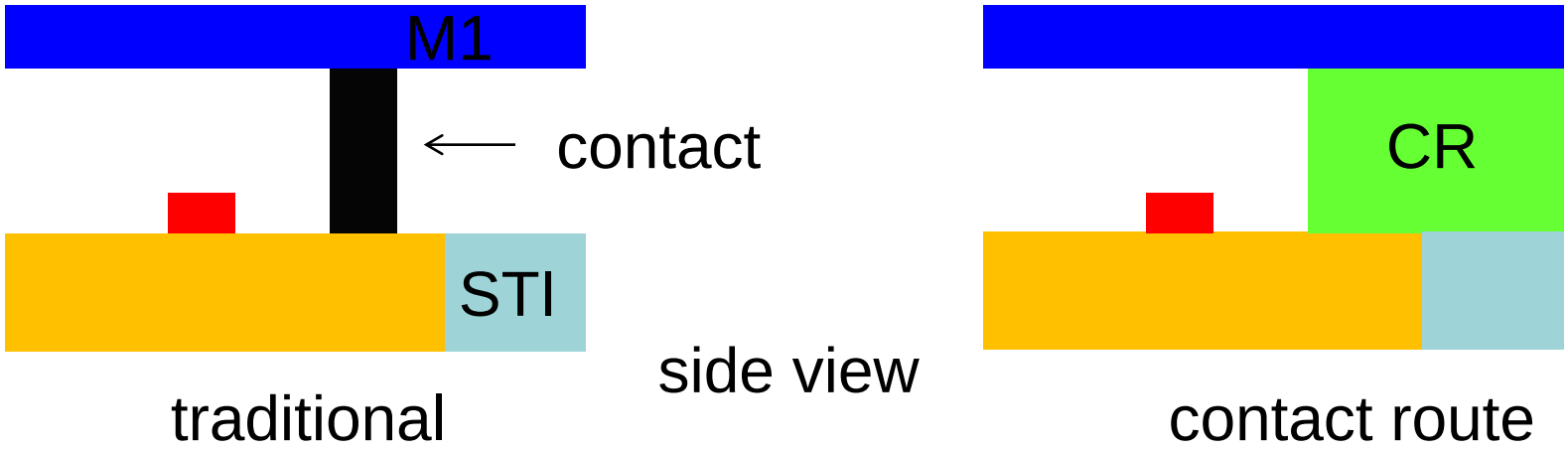
A New Layer for Routing

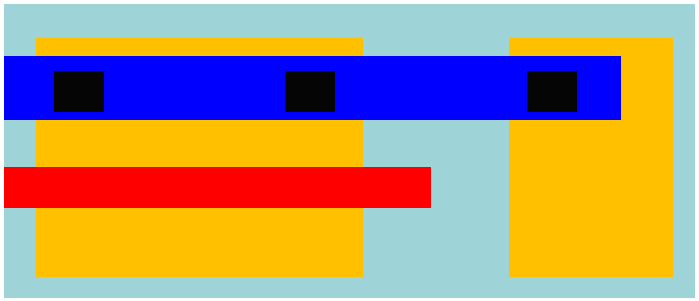
- We can use contact-level routing as an interconnect



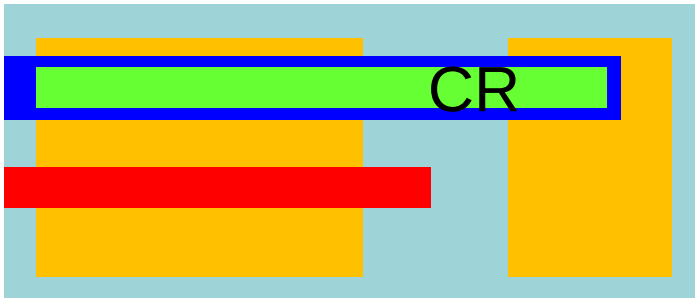
- Contact route (CR) provides a direct connection to M1, diffusion, or polysilicon in this work
- Height of contact ~3x height of M1
  - → ~1/3 lower routing resistance than M1 if copper
  - → ~2x larger if tungsten; but can be in parallel
  - → negligible contact resistance if routing is in CR

Conversion to Contact Routes

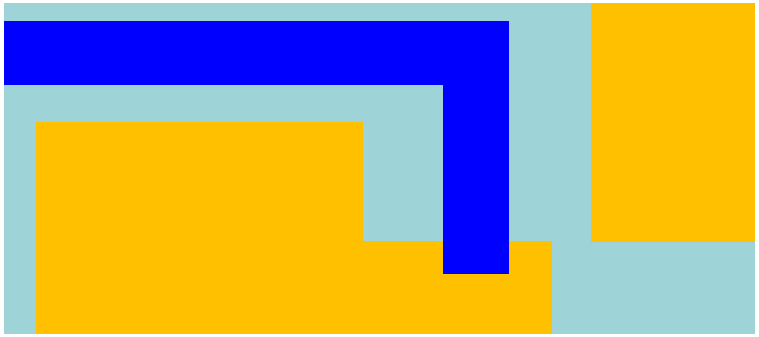
- If M1 connects multiple active islands, utilize contact route below M1

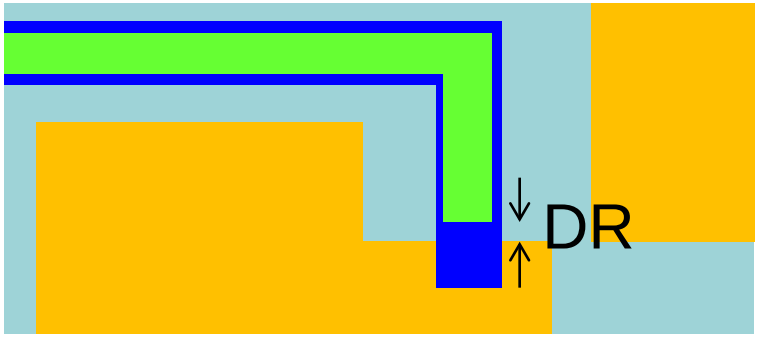


layout view



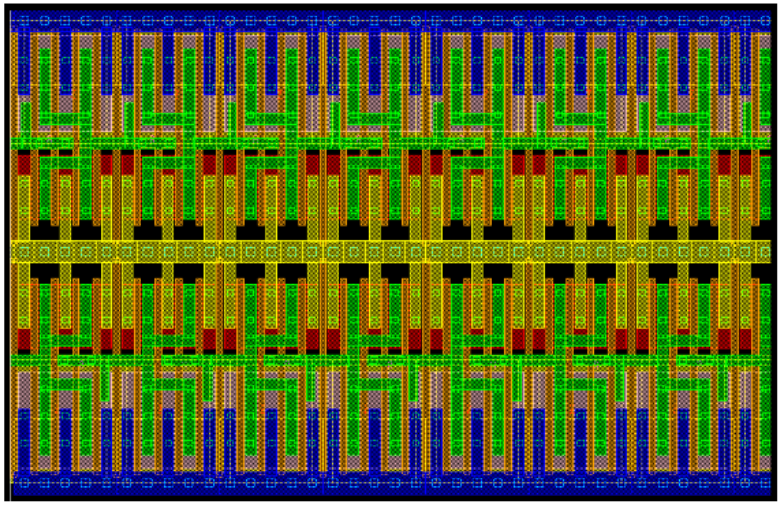
- If M1 does not overlap active or gate areas, utilize contact route below M1

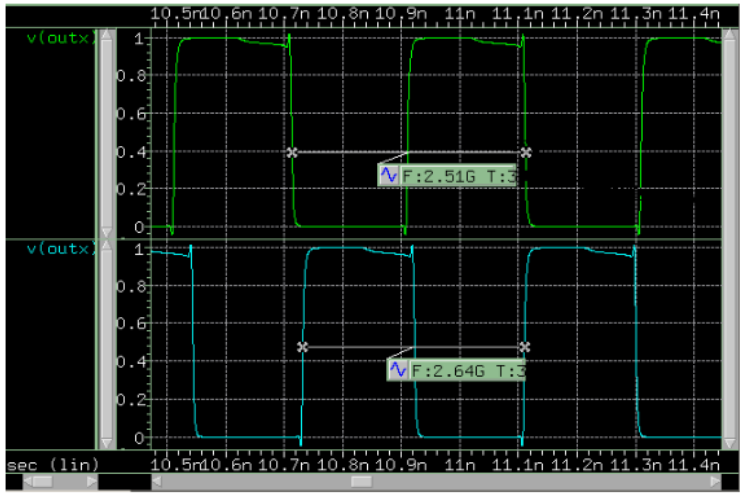




Performance due to Contact-Level Routing

- We compare improvement due to contact-level routing of 47 stage fanout-1 4x inverter ring oscillator assuming tungsten contact routes





- We achieve 4.92% frequency increase with contact-level routing

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Conclusions for 3-2-1 Contact

3. Our test structures and characterization enable accurate models and avoid double counting of contact resistance effect due to RC extraction

2. We provide a method for quick library port to contact-level routing

1. We analyze contact bars and contact-level routing impact on circuit performance; we obtain 4.92% improvement with contact-level routing