On-Chip EM-Sensitive Interconnect Structures

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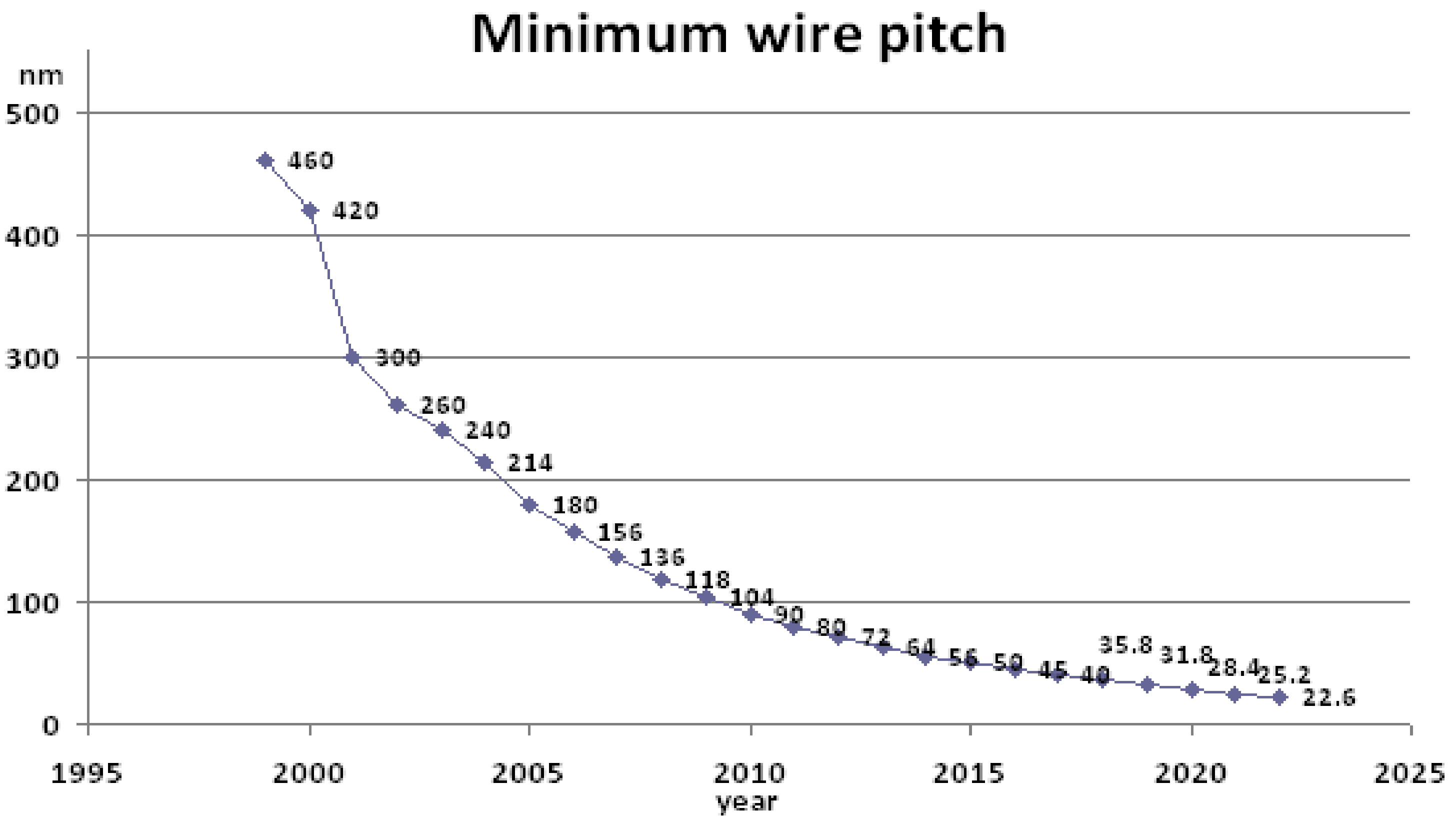
Outline

- **Introduction to EM**
- EM related effects
- EM on tri-state bus
- EM on non-tree clock
- Conclusions

Introduction to EM



- Wire size shrinking
- Circuit complexity increasing

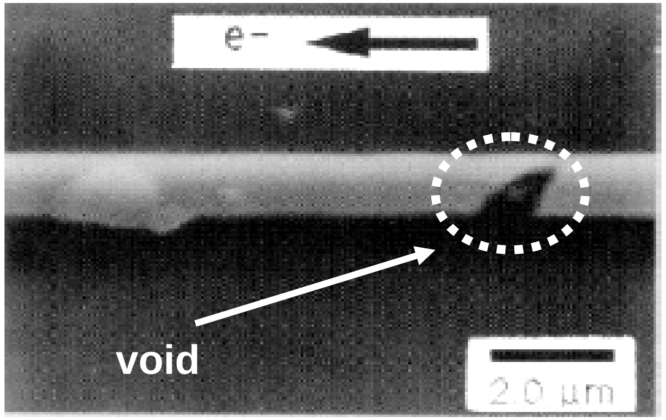
⇒ **Current density increase**

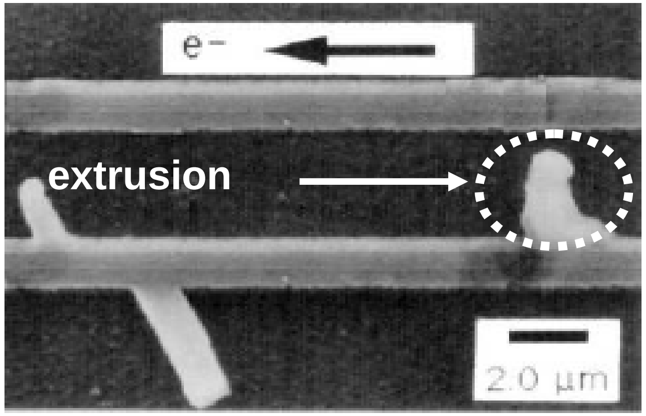
Source: ITRS

Introduction to EM

- Electromigration: the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms

- EM failure
  - Void
  - Extrusion





Source: Wikipedia & Nix 1992

Introduction to EM

- EM lifetime projection: Black's equation

$$MTTF = \frac{A}{J^n} \cdot \exp(\frac{E_a}{k \cdot T})$$

  - n — current exponent, typical value 1~2
  - E_a — activation energy, typical value 1.2eV

- Note: the model is abstract, not based on a physical model, but flexibly describes the failure rate dependence on the temperature, the electrical stress, and the specific technology and materials

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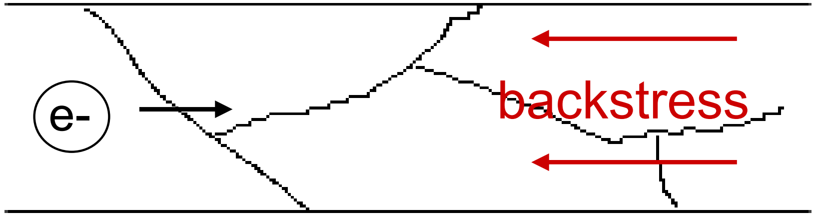
EM Related Effects

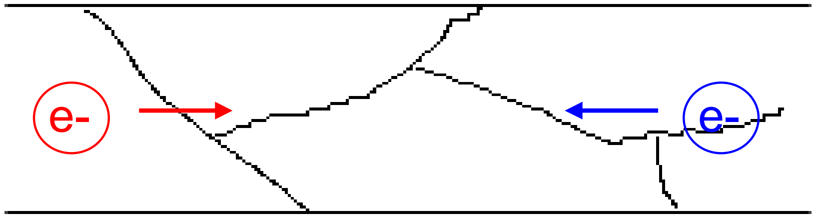
- Blech length
  - $L < L_{Blech} \Longrightarrow$ immortal to EM
  - $j \cdot L < (j \cdot L)_c = \text{constant}$



  - Caused by EM-induced backstress
  - Typical value 10s of μms

EM Related Effects

- Self-healing
  - Caused by currents in opposite directions



  - Average current recovery model

$$J_{EM,eff} = J_{ACR} = \frac{1}{T}[\int_0^T |j_+(t)|\,dt - \gamma \int_0^T |j_-(t)|\,dt]$$

    - γ — recovery coefficient, typical value 0.8~1

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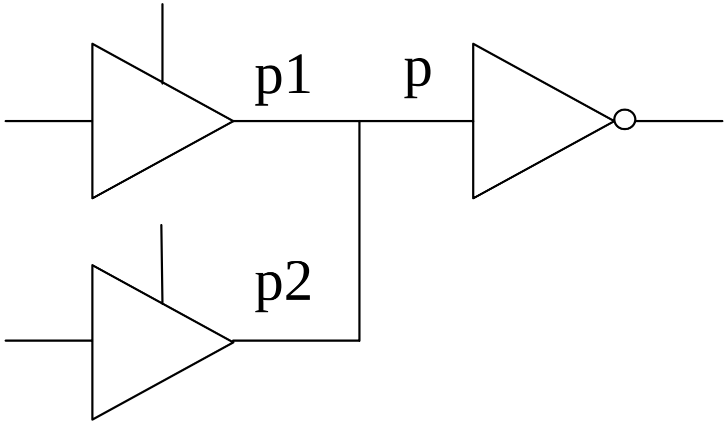
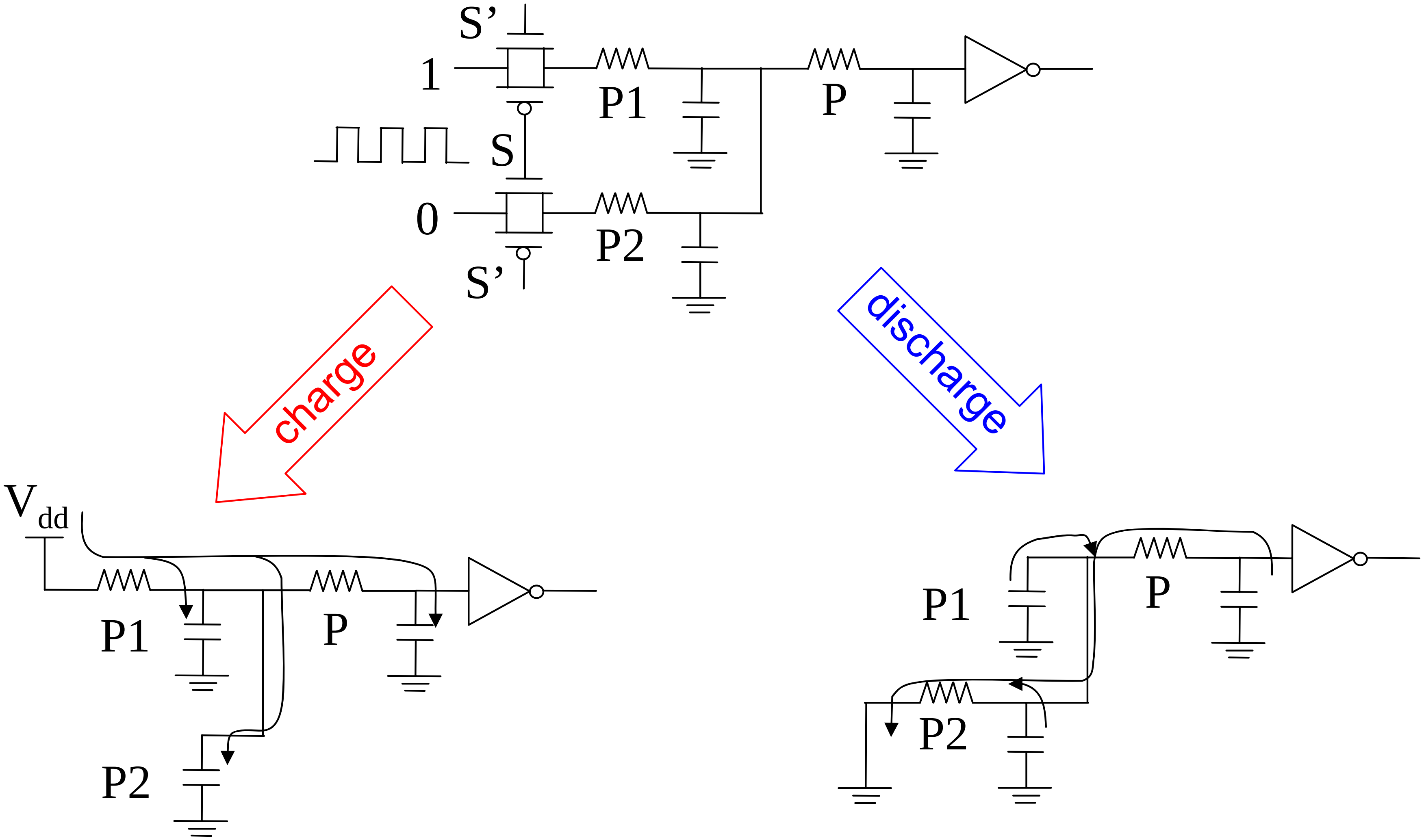
EM on Tri-State Bus

- AC balanced condition
  - Most signal lines are in AC balanced condition: carry both positive and negative current, waveforms do not have to be the same, but the overall charge is close to zero

- Note: AC balanced condition is broken, if there exist different charge and discharge paths.

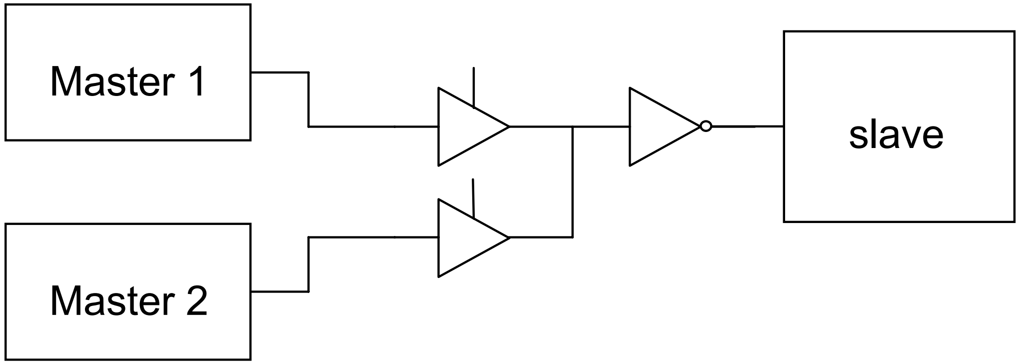


EM on Tri-State Bus



EM on Tri-State Bus

- Tri-state bus



- Circuit operation
  - probability estimation: *m* is a critical cycle number such that if during *N* cycles, for *m* or more cycles current is unidirectional, interconnect EM failure occurs

$$P_{\geq mu} = P_{Nu} + P_{(N-1)u} + \ldots + P_{mu} = \sum_{i=m}^{N} P_{iu}$$

$$P_{Nu} = 2[(f_{s1} \cdot f_{m10} \cdot f_{s2} \cdot f_{m21})^{N/2} + (f_{s1} \cdot f_{m11} \cdot f_{s2} \cdot f_{m2})^{N/2}]$$

EM on Tri-State Bus

- Wire parasitic parameters

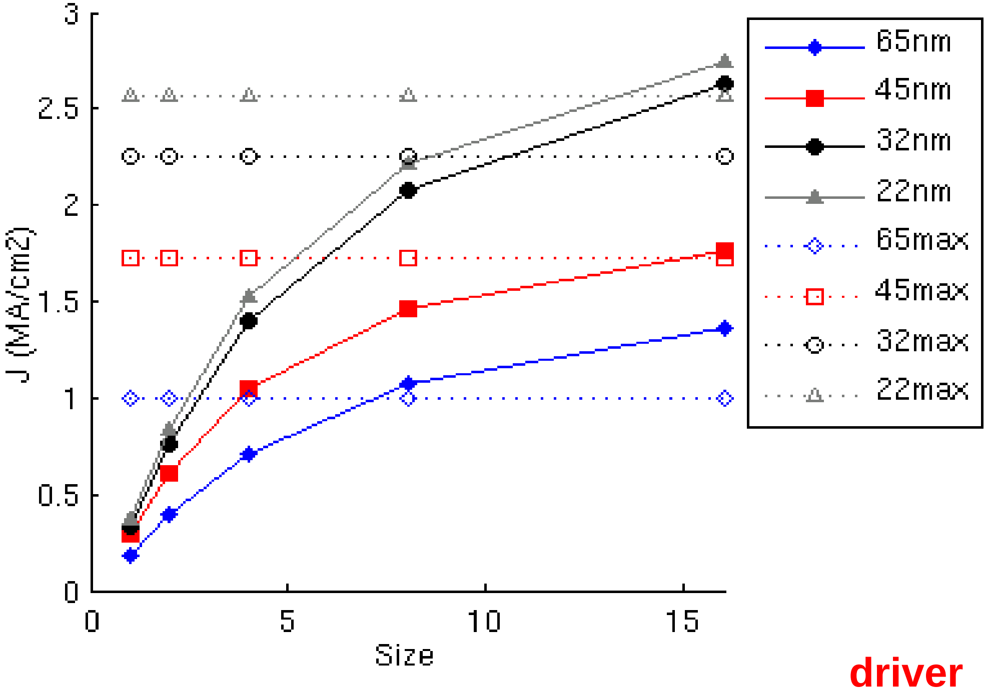
Param Tech	w (nm)	h (nm)	r(ohm/um)	c(fF/um)	f(GHz)	T(°C)
65nm	130	104-117	3.3-3.6	0.18-0.2	0.25-1.5	105
45nm	90	72-81	7.7-8.7	0.16-0.18		
32nm	65	54-61	17.6-19.9	0.15-0.18		
22nm	45	37-42	41.5-47.1	0.13-0.16		

- Sweep parameters
  - Driver size
  - Frequency
  - Wire width
  - Dielectric constant

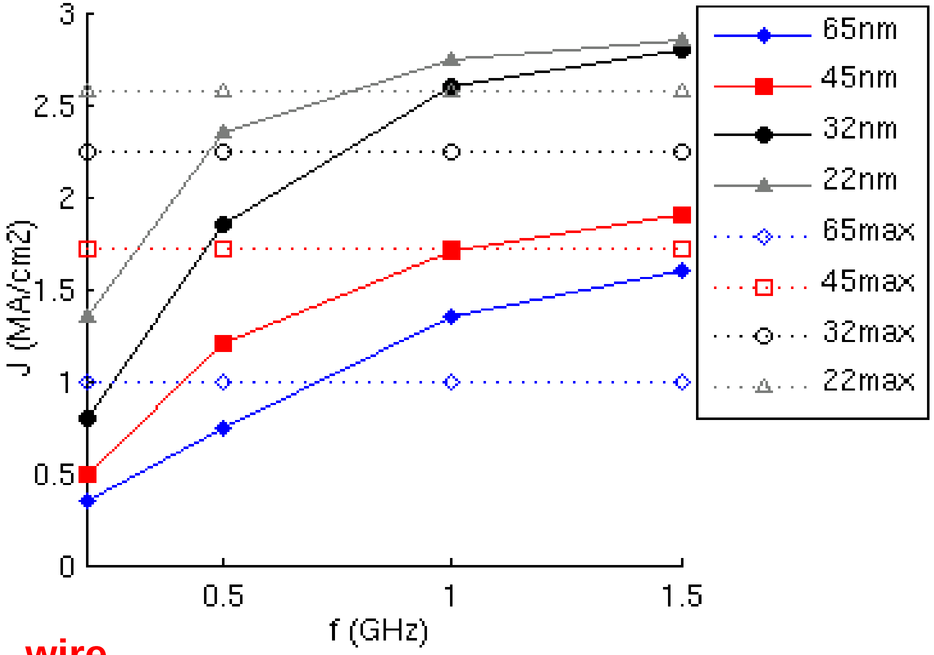
Source: PTM

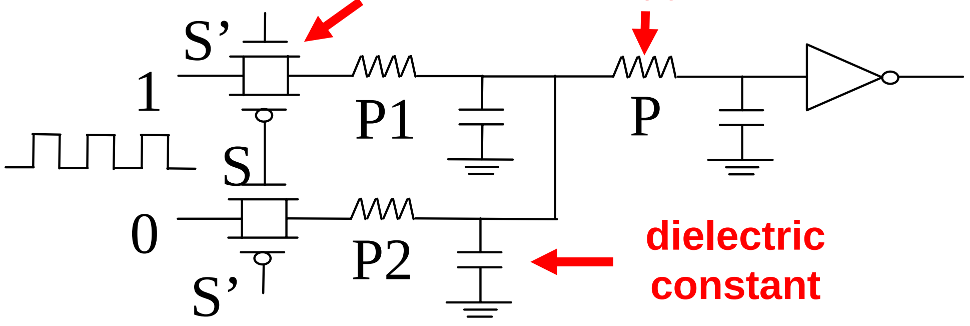
EM on Tri-State Bus

- J versus **driver size**



- J versus **circuit frequency**





driver size

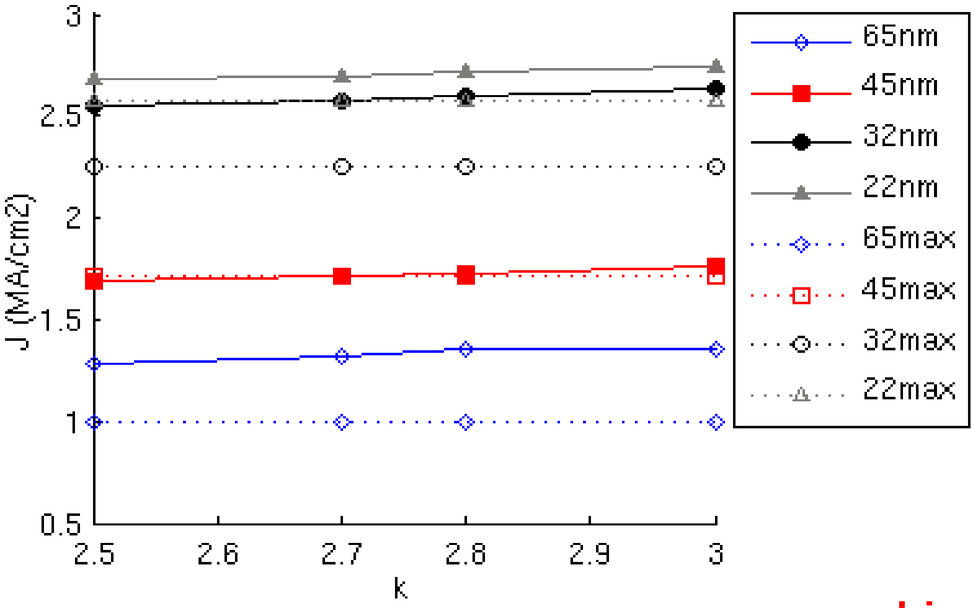
wire width

circuit frequency

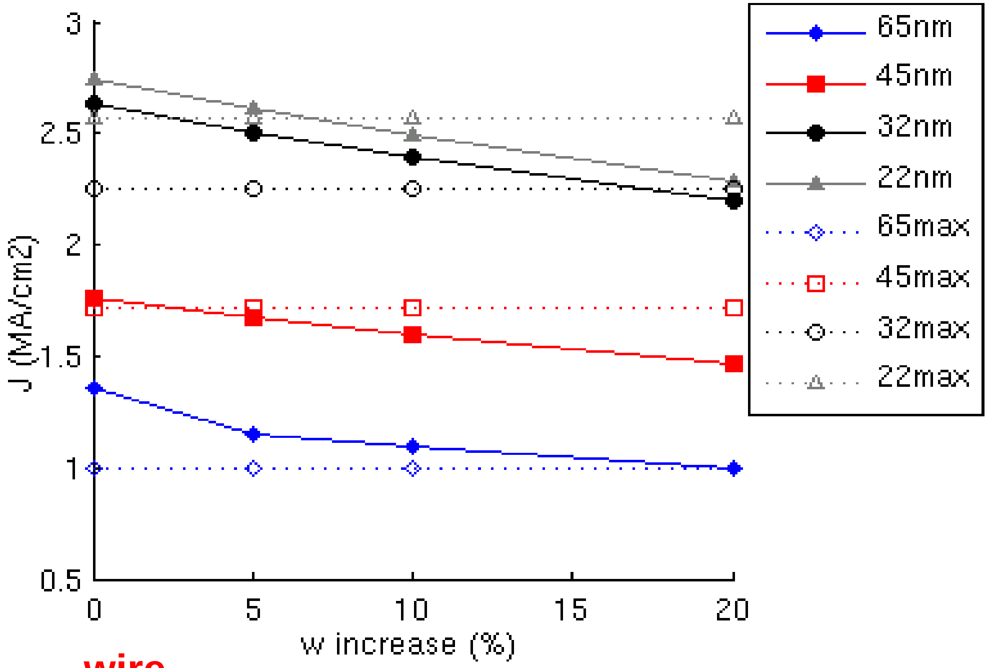
dielectric constant

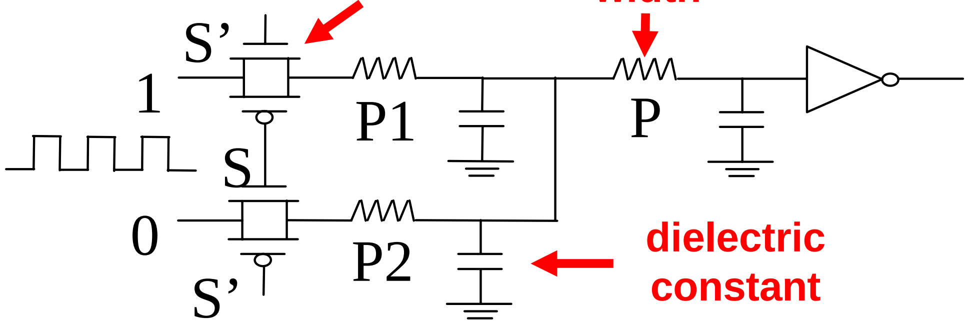
EM on Tri-State Bus

- J versus **dielectric constant**



- J versus **wire width**





driver size

wire width

circuit frequency

dielectric constant

EM on Tri-State Bus

- Traditional trade offs
  - Wire width increase: simple but efficient compared to other trade offs

- New technology
  - CoWP coating
    - increase E_a at metal/cap interface
    - improve EM up to 2x
    - save additional wire budget

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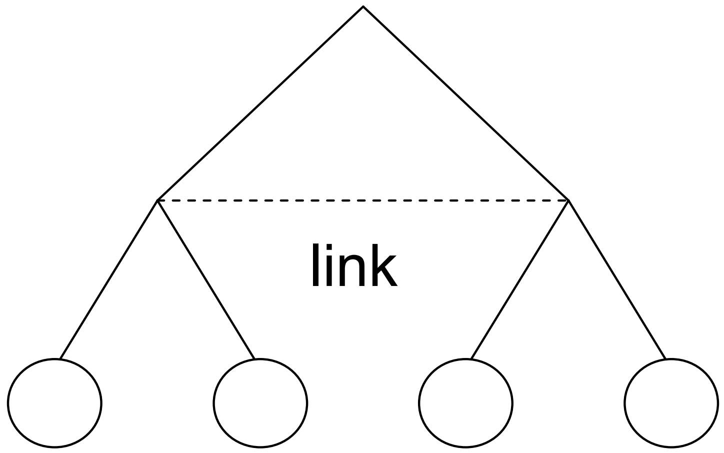
EM on Non-Tree Clock



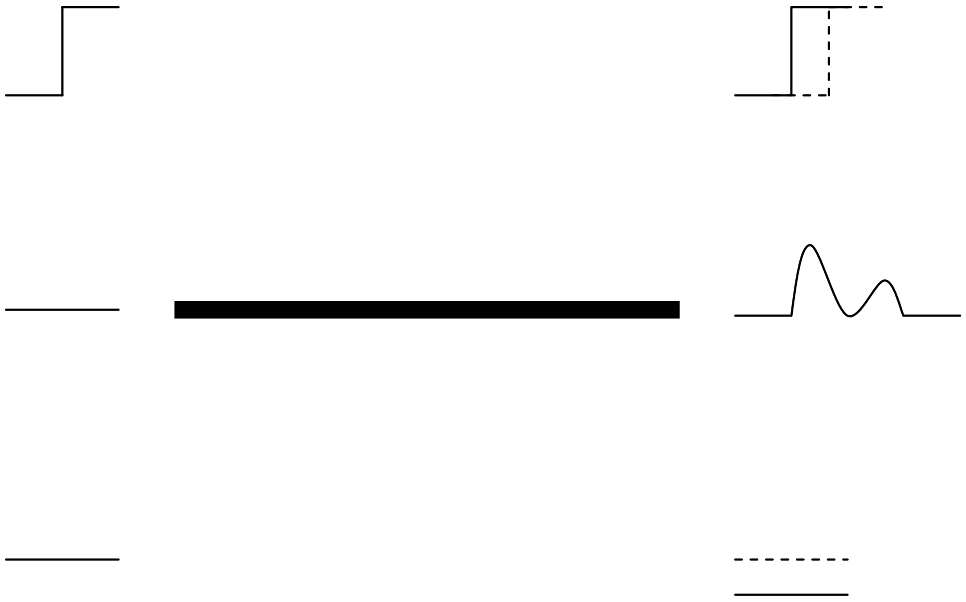
- Advantage
  - Lower skew
  - Variation tolerant (timing)

- Disadvantage
  - Extra wire length
  - Reliability concerns

(connect wires with different voltage potentials)

EM on Non-Tree Clock

- Sources of voltage potential difference
  - Clock skew
  - Power noise
  - Thermal effects



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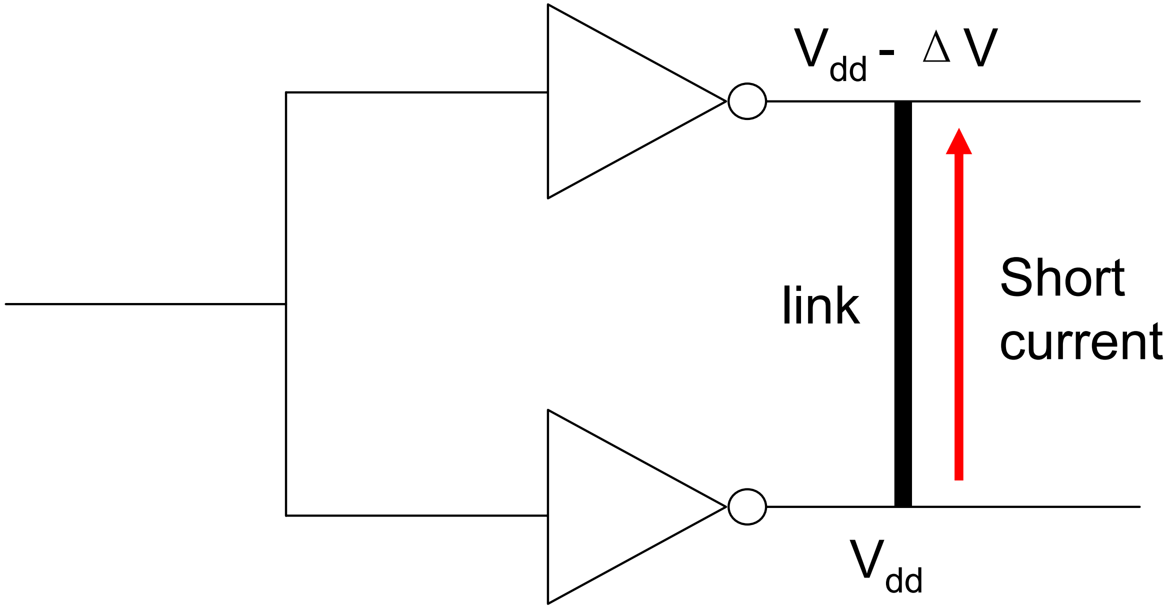


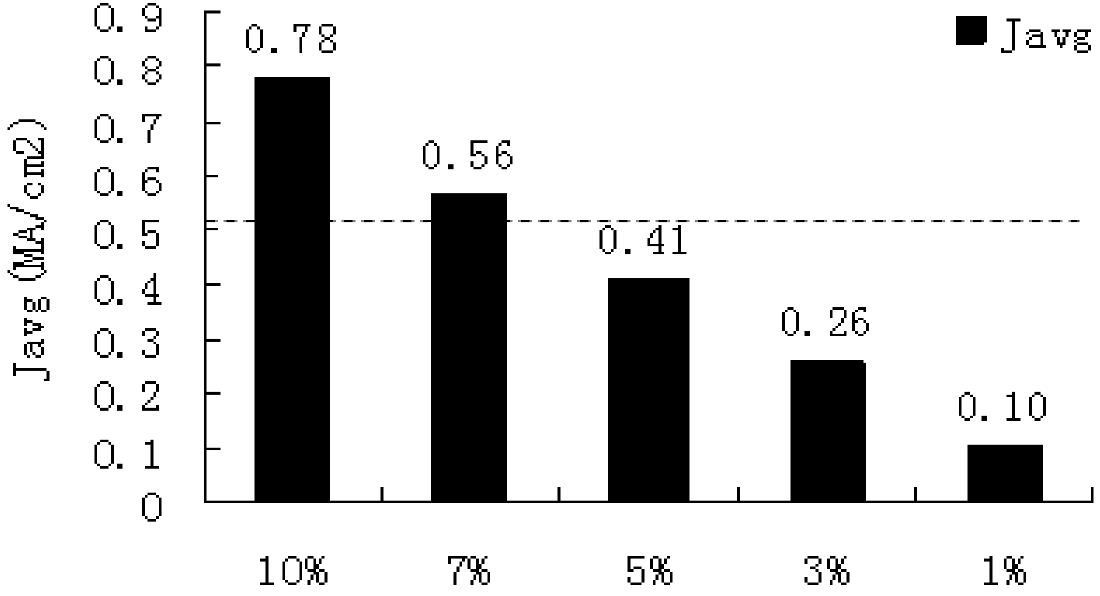
- Link failure
  - doest not necessarily cause fatal malfunction but degrades performance and eliminates any advantage derived from the link

EM on Non-Tree Clock

- Non-tree/tree

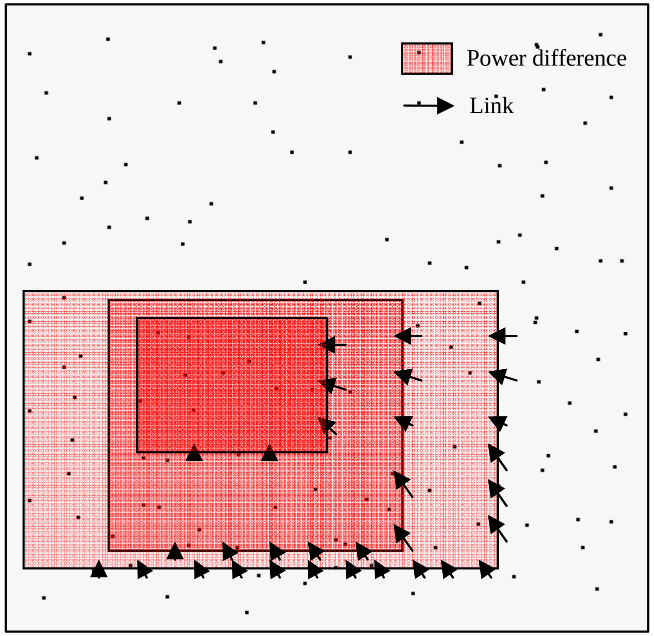
Test case	worst J_{avg} (tree) (A/cm^2)	worst J_{avg} (non-tree) (A/cm^2)	non-tree/tree ratio
r1	8.16E02	1.50E04	18x
r2	1.24E02	2.92E03	23x
r5	2.85E02	1.89E04	66x
s13207	6.89E02	9.11E04	132x
s38584	1.26E03	7.34E04	58x

- Power noise margin



EM on Non-Tree Clock

- Links in non-tree clock across boundaries of areas with power supply difference



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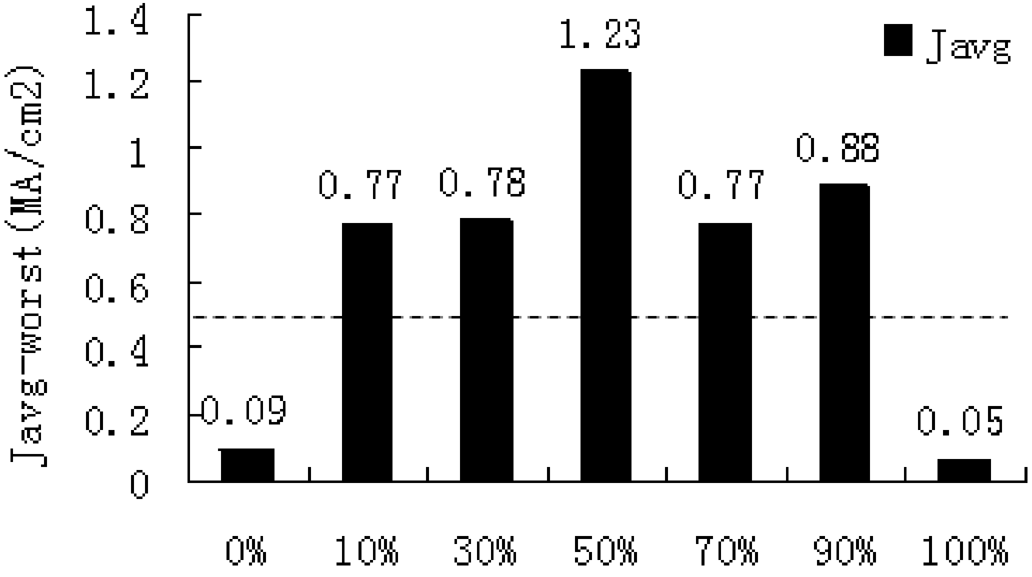

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Conclusions

- Summary
  - EM—dominant reliability effects
  - EM-sensitive structures
    - Tri-state bus
    - Non-tree clock
  - EM trade offs
- Future work
  - Study on EM technological solution
  - EM-aware design

Thanks for your attention!

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