Taking semiconductors to the next level

Tier Logic 3D FPGA™ & 3D ASIC™
Worlds first unified 3D IC design platform

Peter Suaris, Tier Logic Inc.
SLIP, June 2010
2D FPGA background

- Large Silicon area to support programming
  - Limiting CR – hurts routing & logic efficiency
- Architecture trade off – channel wires vs. CRAM
  - Process metal pitch $\rightarrow$ fixed wires per logic area

$LO = Logic + FF \quad CR = Config \ RAM \quad RO = routing \ (MUX \ & \ buffers)$
3D Product concepts

• 2D FPGA – poor area, cost, power, speed

• 3D FPGA™ – better area, power, cost, speed
  – Same placement / same die 3D ASIC™
  – One design – FPGA/ASIC options
“Bitstream” timing closure

TierFPGA
• TFT SRAM

TierASIC
• Metal ROM

MultiASIC™
• TFT MUX

3D Static Control

Dynamic Signals

One bitstream = identical timing = deterministic

Base die
Unified process

- TFT SRAM over CMOS
  - FPGA fabric / FPGA tools
  - Temperature < 400 °C

- Metal ROM over CMOS
  - FPGA fabric / FPGA tools
  - “Bitstream” custom M9
Process technologies

- TFT SRAM over CMOS
  - FPGA fabric / FPGA tools
  - Temperature < 400 °C

- Metal ROM over CMOS
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TFT SRAM latches

- Static circuits
- $V_T$ not critical
- Low power
Channel wires

- **2D FPGA dilemma**
  - More CR to reduce N
  - More CR – increases cell Area – no gain

- **3D FPGA benefit**
  - CR in 3D – more area available for CR
  - More CR – reduce N

- **3D FPGA routing**
  - Larger logic clusters to reduce IO
  - More CR to use less wires
Routing architecture

• Logic cell area = 1
  – Wires / area = N
  – RO per wire = 0.6 / N
  – Area = 1 = LO + CR + RO₁
  – LO = 12.5%
  – LO efficiency ~ ¼ of ASIC

No CR 2D FPGA cell area = f

Area:
CR = CRAM LO
= Logic
RO = Routing

• New logic cell area = f
  – Wires = N * f ( < N )
  – RO₂ = 0.6 * f ( < 0.6 )
  – Area = f = LO + RO₂
  – f = 0.313
  – LO = 40% → 3.2x better
  – More CR for ~ N/3 wires
Logic efficiency

- **2D FPGA dilemma**
  - More IO for higher LO efficiency
  - More IO – more CR – increase area – no gain

- **3D FPGA benefit**
  - CR in 3D – more IO & CR – better LO

- **3D FPGA logic**
  - Larger clusters & better packing
3D IC for FPGAs

- Fine Grain for logic + Course Grain for routing
- Routing breakthroughs
  - One tool for FPGA and ASIC
  - “Bitstream” style of timing closure
  - More CR to reduce channel wires needed
- Logic breakthroughs
  - More IO & CR to improve logic packing
- Standard front end tools
  - Leverage existing synthesis tools & IP
  - Push button – no new learning
Improving gate density

• Approach ASIC gate density
• Improved mobility switch fabric

3D FPGA™
Low ROI IC’s

2D FPGA

Tru3D™
FPGA
ASSP / ASIC

Competition
Tier Logic 2010
Tier Logic 2012
Competitive evolution

- Multi-faceted technology evolution
  - 3.5x 3D FPGA
  - 7x Tru3D
- Programmability – as needed – iterative
- Fixed function – when satisfied
- All future ICs will need programmability
- 56 issued patents
4LUT gate density

**2D FPGA 4LUTs follow Moore’s Law**
- 110 /mm² 2000 (180 nm)
- ~4500/mm² 2013 (20nm)

6 nodes ~ 40x

**3D offers higher 4LUTs**
- 16k /mm² 2013 (28 nm)
Summary

- Unified IC design for FPGA & ASIC
  - Beyond process scaling
  - “Bitstream” concept to 3D ICs
- Worlds first monolithic 3D FPGA
  - Same “netlist / placement / base-die” → 3D ASIC
  - 3D FPGA/ASIC – available 2010
- Augment programmability to ASIC density
  - Tru3D FPGA/ASIC – available 2012
- *Tier Logic: taking semiconductors to the next level*