Efficient Tiling Patterns for Reconfigurable Gate Arrays
(or Why you shouldn't be driving in Manhattan ?)

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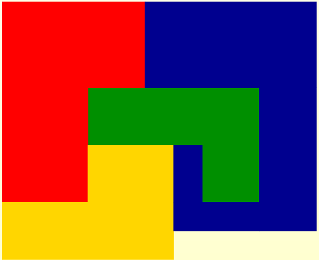
Newcastle, UK

Plan

- Intuition
- First Principles
- Evaluation Method
- Tiling Patterns
  - Octagonal Tiling
  - Hexagonal Tiling
  - Hierarchical Tiling
- Comparison
- Layout Schemes
- Depopulation Schemes
- True Length Estimation
- Conclusion & Future Research
- Questions

Intuition: The Four Color Theorem

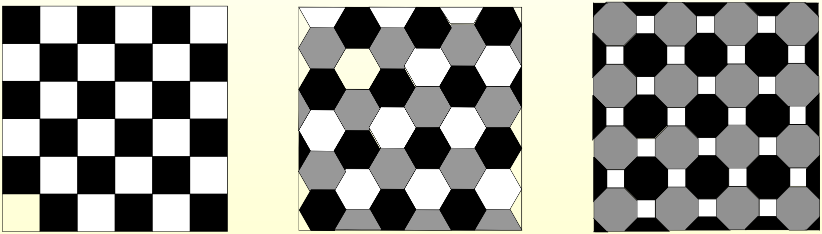
(a) The Map of Europe in Four Colors



(b) No more than Four Mutual Neighbours in a plane

Figure 1: The Four Color Theorem.

Intuition: Tiling patterns



(a) Square (b) Hexagonal (c) Octagonal

Figure 2: More Mutual Neighbours The Better

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First Principles: Measurement Units

- Hops = No. of constituting segments (always integer)
- True Length = True interconnect length in metric units

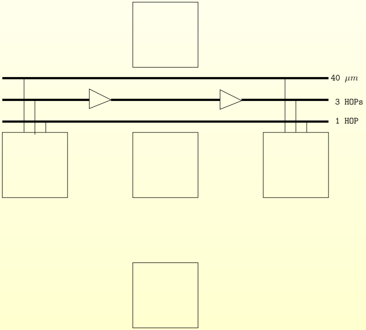

Figure 3: Hops and true length

First Principles: Rent's Rule

$$T = tB^p, \quad 0 \le p \le 1, \text{ where:} \tag{1}$$

- T is the number of terminals of the partition,
- B is the number of elementary blocks in that partition,
- t is the Rent coefficient, *i.e.* the average number of terminals par elementary block,
- p is the Rent exponent.

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- T is the number of terminals of the partition,
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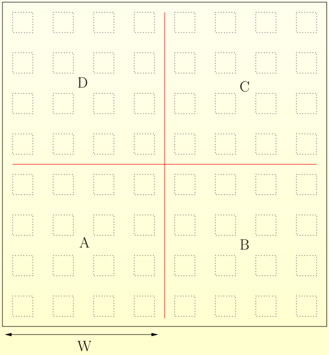
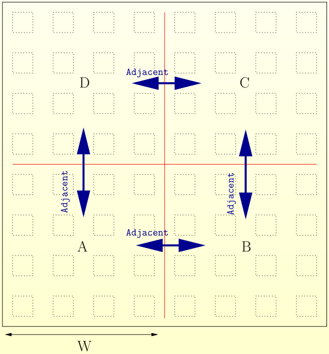
- p is the Rent exponent.
- Hereafter we will represent each user netlist as a triplet $\langle t, p, B \rangle$

First Principles: Donath Revisited



$$\overline{n_k} = \alpha t B(1 - 4^{p-1})4^{k(p-1)}$$
$$r = |x_1 - x_2| + |y_1 - y_2|$$

First Principles: Donath Revisited



$$r_{adj} = \frac{1}{W^4} \sum_{i_A=1}^{W} \sum_{j_A=1}^{W} \sum_{i_B=1}^{W} \sum_{j_B=1}^{W} (W + i_A - i_B + |j_A - j_B|)$$

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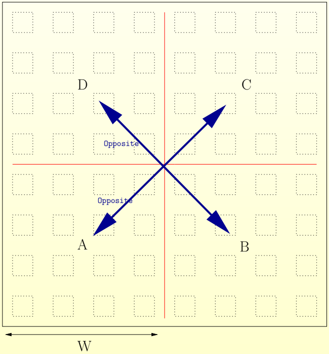

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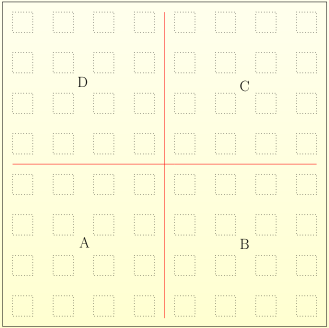
$$r_{opp} = \frac{1}{W^4} \sum_{i_A=1}^{W} \sum_{j_A=1}^{W} \sum_{i_C=1}^{W} \sum_{j_C=1}^{W} [(W + i_A + j_A - i_C - j_C]$$

$$\overline{r_k} = \frac{4\overline{r_{adj}} + 2\overline{r_{opp}}}{6}$$

First Principles: Donath Revisited



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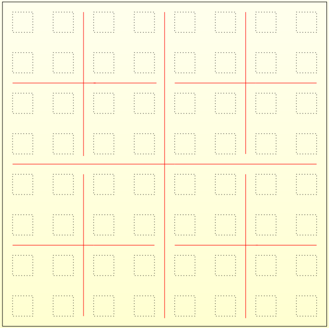

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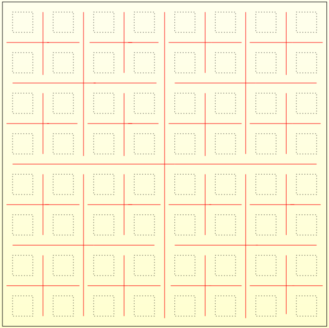

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$$\overline{n_k} = \alpha t B(1 - 4^{p-1}) 4^{k(p-1)}$$

$$r = |x_1 - x_2| + |y_1 - y_2|$$

$$L_{netlist} = \overline{n_0} \times \overline{r_0} + \overline{n_1} \times \overline{r_1} + \overline{n_2} \times \overline{r_2}$$

First Principles: Equivalence of Wire Length & Wire Flow

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$$\text{Total Interconnect length} = \text{No. of occupied segments/tile} \times \text{No. of Tiles}.$$

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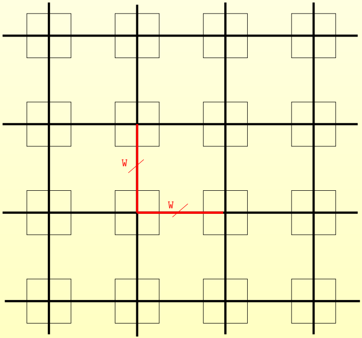

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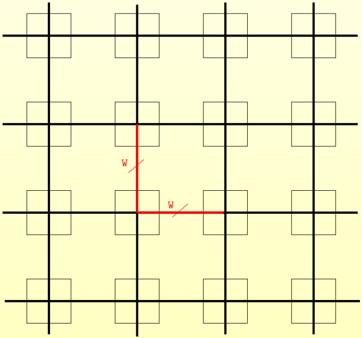

Manhattan Grid

$$L_{hops} = 2w \times B\,.$$
$$\overline{w} = \frac{L_{wire}}{2B}\,.$$

Plan

Evaluation Method

- First we calculate the point-to-point distance on the tiling pattern.

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Evaluation Method

- First we calculate the point-to-point distance on the tiling pattern.
- Next we calculate the Total interconnect length for a given user netlist $< t, p, B >$
- We calculate the Average channel width required
- ➙ We count the no. of switches for that channel width

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Tiling Patterns: Octagonal

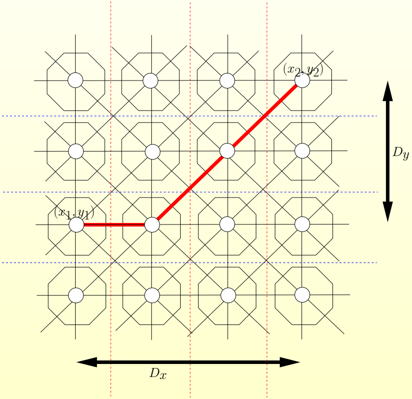
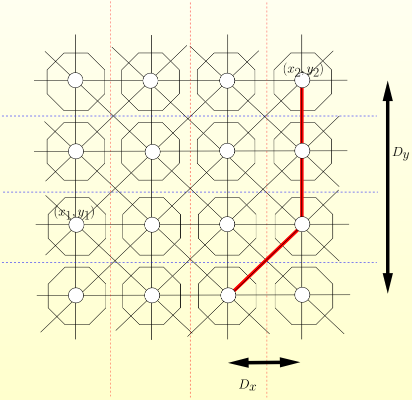


Figure 5: Distance Between two points in an Octagonal grid

$$D_x = |x_1 - x_2|, \qquad D_y = |y_1 - y_2|$$

$$r \quad = \quad D_x + D_y - D_x \qquad D_y \geq D_x$$

Tiling Patterns: Octagonal



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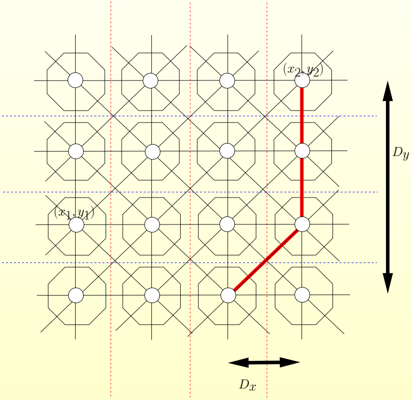
Tiling Patterns: Octagonal



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$$D_x = |x_1 - x_2|\,, \qquad D_y = |y_1 - y_2|$$

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$$r \quad = \quad D_y + D_x - D_y \qquad D_x \geq D_y$$

Octagonal Grid

$$r = \frac{1}{2}\left(D_x + D_y + \left|D_x - D_y\right|\right)$$

Tiling Patterns: Octagonal

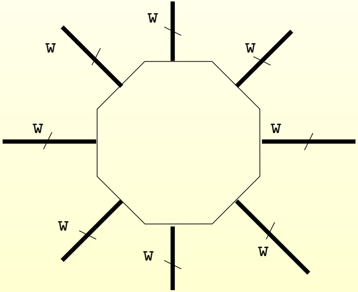


Figure 6: No. of switches Required

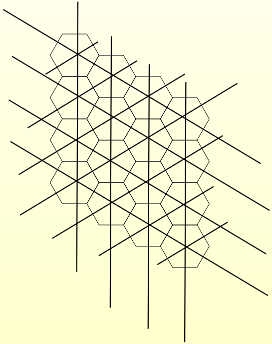
Octagonal Grid

$$\text{No. of Switches} = C_2^N \times w^2$$
$$\text{No. of Switches} = 28 \times w^2$$

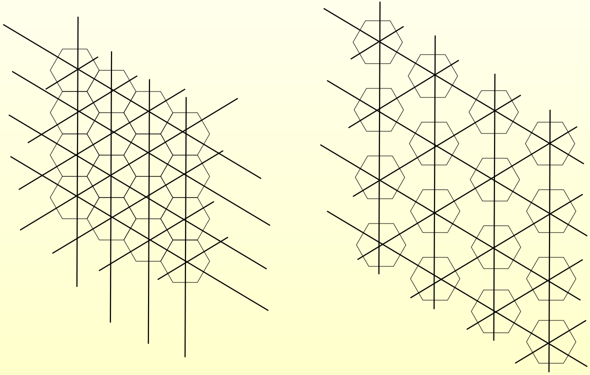
Octagonal Grid

$$L_{hops} = 4w \times B \,.$$
$$\overline{w} = \frac{L_{wire}}{4B} \,.$$

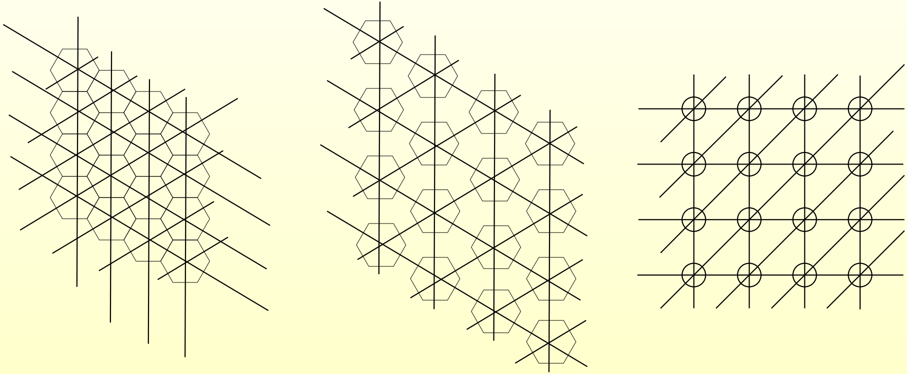
Tiling Patterns: Hexagonal



Tiling Patterns: Hexagonal



Tiling Patterns: Hexagonal



Point-to-Point Distance in Hops remains the same across Transformations

Tiling Patterns: Hexagonal

$$D_x = |x_1 - x_2|\,, \qquad D_y = |y_1 - y_2|$$

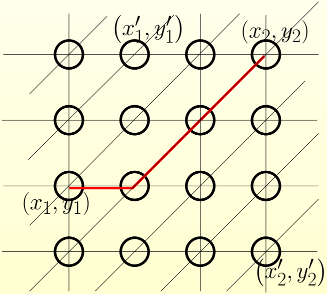


Figure 7: Distance Between two points in an hexagonal grid

$$r = \frac{1}{2}\left(D_x + D_y + |D_x - D_y|\right) \qquad (x_2 \geq x_1, y_2 \geq y1)$$

$$(x_2 \leq x_1, y_2 \leq y1)$$

Tiling Patterns: Hexagonal

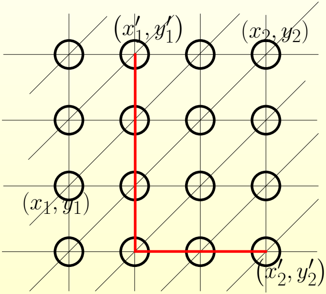


Figure 7: Distance Between two points in an hexagonal grid

$$D_x = |x_1 - x_2|\,, \qquad D_y = |y_1 - y_2|$$

$$r = \frac{1}{2}\left(D_x + D_y + |D_x - D_y|\right) \qquad (x_2 \geq x_1, y_2 \geq y1)$$
$$(x_2 \leq x_1, y_2 \leq y1)$$
$$= D_x + D_y \qquad \textit{otherwise}$$

Tiling Patterns: Hexagonal

$$D_x = |x_1 - x_2|, \qquad D_y = |y_1 - y_2|$$

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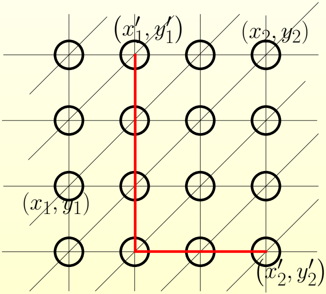

Figure 7: Distance Between two points in an hexagonal grid

Hexagonal Grid

$$2r = \left(1 + \frac{(x_2 - x_1)(y_2 - y_1)}{|x_2 - x_1|\,|y_2 - y_1|}\right)\frac{1}{2}\left[(D_x + D_y) + \left|D_x - D_y\right|\right] + \left(1 - \frac{(x_2 - x_1)(y_2 - y_1)}{|x_2 - x_1|\,|y_2 - y_1|}\right)\left[D_x + D_y\right]$$

Tiling Patterns: Hexagonal

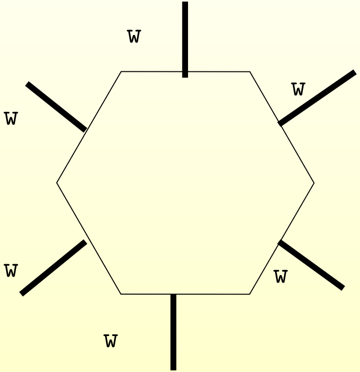

Figure 8: No. of switches Required

Hexagonal Grid

$$\text{No. of Switches} = C_2^N \times w^2$$
$$\text{No. of Switches} = 15 \times w^2$$

Hexagonal Grid

$$L_{hops} = 3w \times B\,.$$
$$\overline{w} = \frac{L_{wire}}{3B}\,.$$

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Comparison

Parameter	Square	Hexagonal	Octagonal
Total Interconnect Length	1	0.85	0.69

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Parameter	Square	Hexagonal	Octagonal
Total Interconnect Length	1	0.85	0.69
Average Channel Width	1	0.56	0.35

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Parameter	Square	Hexagonal	Octagonal
Total Interconnect Length	1	0.85	0.69
Average Channel Width	1	0.56	0.35
No. of Switches/SwitchBox	1	0.78	0.57

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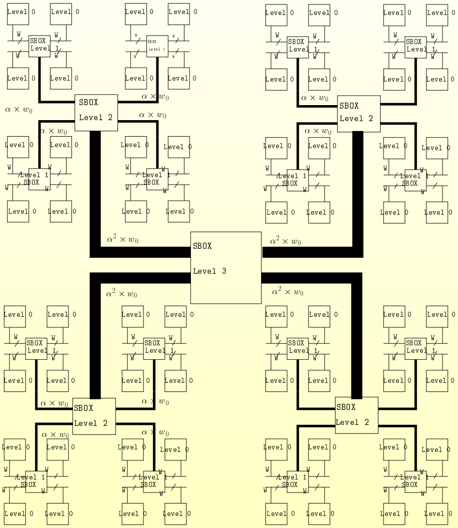
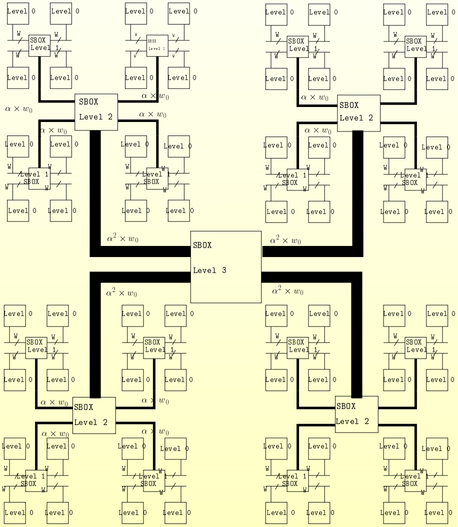
Butterfly Fat Tree



- arity A: no of branches

Butterfly Fat Tree



- arity A: no of branches
- α : ratio of channel width of a level to it's next level

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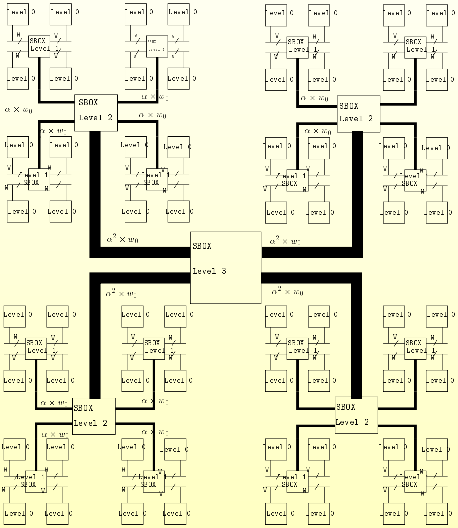
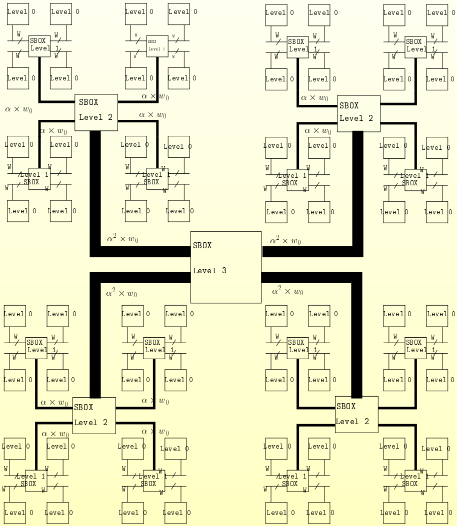


- arity A: no of branches
- α : ratio of channel width of a level to it's next level
- → and w_k as the channel width at level k.

$$\alpha = \frac{w_{k+1}}{w_k}$$

Butterfly Fat Tree



- arity A: no of branches
- α : ratio of channel width of a level to it's next level
- and w_k as the channel width at level k.

$$\alpha = \frac{w_{k+1}}{w_k}$$

→ Point to point distance between two points between two adjacent partitions at level k $r = (2k + 1)$

Comparison

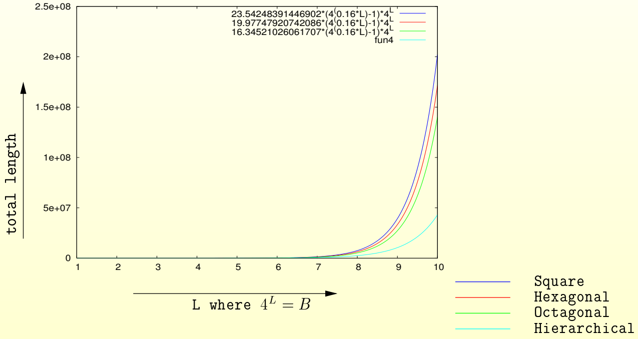


Figure 10: Total Interconnect length for different `Tiling Patterns` for a given user netlist $\langle 4, 0.66, 4^L \rangle$

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Layout Schemes: Hexagonal

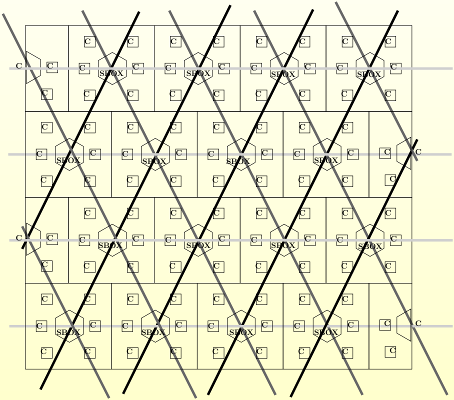

Figure 11: Hexagonal FPGA Layout Scheme

Layout Schemes: Hexagonal with 45° lines

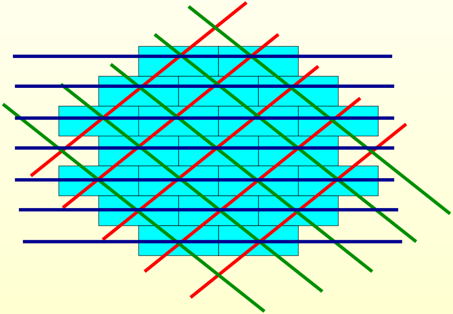

Figure 12: Standard Processes support 45° metal lines

Layout Schemes: Octagonal

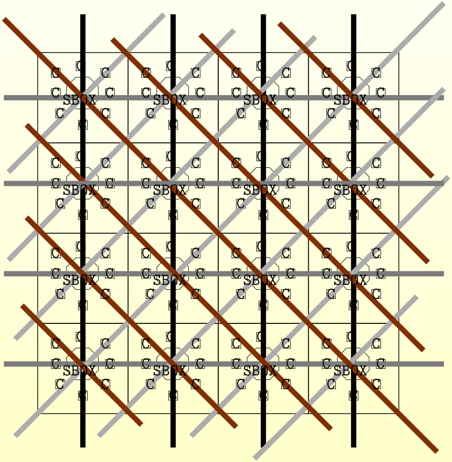

Figure 13: Octagonal FPGA Layout Scheme

Plan

Depopulation Schemes

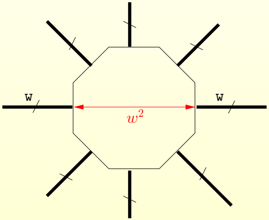

Figure 14: No. of switches are more than the Channel Capacity

➞ No. of switches between two channels (W^2) $>>$ Channel Capacity (W)

Depopulation Schemes

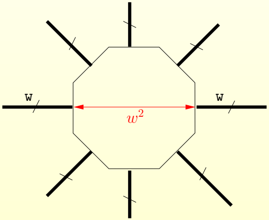

Figure 14: No. of switches are more than the Channel Capacity

- No. of switches between two channels (W^2) >> Channel Capacity (W)

➞ Let's Depopulate the X-Bar to Disjoint Switchbox.

Depopulation Schemes

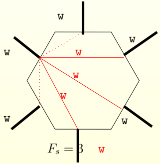

Figure 15: Eliminating Unused connections in Shortest Path

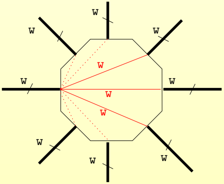

Figure 16: Eliminating Unused connections in Shortest

Hexagonal Grid

$$\text{No. of Switches(X-bar)} = 15 \times w^2$$
$$\text{No. of Switches(Depopulated)} = 9 \times w$$

Octagonal Grid

$$\text{No. of Switches(X-bar)} = 28 \times w^2$$
$$\text{No. of Switches(Depopulated)} = 12 \times w$$

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- Tiling Patterns
  - Octagonal Tiling
  - Hexagonal Tiling
  - Hierarchical Tiling
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- Layout Schemes
- Depopulation Schemes
- True Length Estimation
- Conclusion & Future Research
- Questions

True Length Estimation

Estimated True Length

$$\text{Tot. Interconnect length}(\mu m) = \text{Av. Length per hop}(\mu m/hop) \times \text{Tot. Interconnect Length in Hops(hops)}.$$

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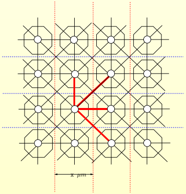

$$\text{Length per hop} = \frac{2 \times \text{Straight hop} + 2 \times \text{Diagonal hop}}{4}$$

$$\text{Length per hop} = 1.207\text{x} \quad \mu m/hop$$

Figure 17: Estimation of True Length in Octagonal grid

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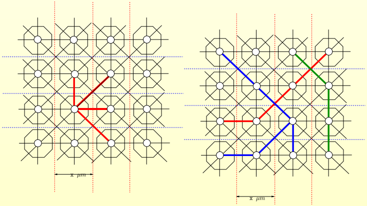

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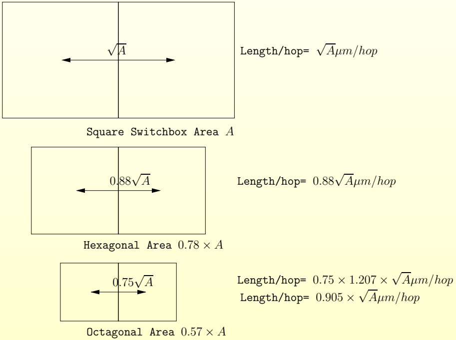
$$\text{Length per hop} = 1.207x \quad \mu m/hop$$

$$\text{Estimated True Length} = 11 \times 1.207x$$

$$\text{Estimated True Length} = 13.377x \quad \mu m$$

$$\text{Actual Length} = 13.484x \quad \mu m$$

True Length Estimation



$$
\begin{aligned}
E(L_{square}) &= 1 \times 1 \times \sqrt{A} \quad \mu m \\
E(L_{Hex}) &= 0.85 \times 0.88 \times \sqrt{A} \quad \mu m \\
&= 0.748\sqrt{A} \quad \mu m \\
E(L_{Octagonal}) &= 0.69 \times 0.905 \times \sqrt{A} \quad \mu m \\
&= 0.63\sqrt{A} \quad \mu m
\end{aligned}
$$

Figure 18: For a given User netlist $< t, p, B >$

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  - Actual CMOS layouts

Thank You

Thank You & Have a Nice Day

(Author's Version of the article with big Mathematical fonts is available at

http://comelec.enst.fr/~chaudhur/Tiles_big.pdf)