SLIP 2006 Technical Program

SATURDAY

WELCOME AND INTRODUCTION (8:30 – 8:45)

Session 1: Prediction of Individual Wire Properties  (8:45 - 10:15) (Chair: Joni Dambre)
- Difficulty of Predicting Interconnect Delay in a Timing Driven FPGA CAD Flow
  V. Manohararajah, G. R. Chiu, D. P. Singh, S. D. Brown (Altera Toronto Technology Center, Canada)
- A Priori Prediction of Tightly Clustered Connections based on Heuristic Classification Trees
  P. Anbalagan, J. A. Davis (Georgia Institute of Technology, USA)
- A Tale of Two Nets: Studies of Wirelength Progression in Physical Design
  A. B. Kahng, S. Reda (University of California at San Diego, USA)

BREAK (10:15- 10:45)

Session 2: Process Variation   (10:45-12:15)   (Chair: Ion Mandoiu)
- An Overview of On-chip Interconnect Variation (Invited Talk)
  L. Scheffer (Cadence Design Systems, USA)
- Generation of Design Guarantees for Interconnect Matching
  A. B. Kahng, R. O. Topaloglu (University of California at San Diego, USA)

LUNCH (12:15 - 14:00)

Session 3: Design for Manufacturability (14:00- 15:00)   (Chair: Lou Scheffer)
- Statistical Analysis and Optimization in the Presence of Gate and Interconnect Delay Variations (Invited Talk)
  C. Visweswariah (IBM T.J. Watson Research Center, USA)

Session 4: Evaluation and Prediction of FPGA Routing Resources (15:00 - 16:00)  (Chair: Mike Hutton)
- Post-Placement Interconnect Entropy: How Many Configuration Bits does a Programmable Logic Device Need?
  W. Feng, J. W. Greene (Actel Corporation, USA)
- The Routability of Multiprocessor Network Topologies in FPGAs
  M. Saldaña, L. Shannon, P. Chow (University of Toronto, Canada)

BREAK (16:00 - 16:30)

Session 5: Prediction and Optimization of Global Interconnect Architectures (16:30 - 18:00) (Chair: Dirk Stroobandt)
- Congestion Modeling for Reconfigurable Interprocessor Networks
  W. Heirman, J. Dambre, J. Van Campenhout (Ghent University, Belgium)
- Modeling and Analysis of the System Bus Latency on the SoC Platform
  Y.-S. Cho, E.-J. Choi, K.-R. Cho (Chungbuk National University, Korea)
- Energy/Area/Delay Trade-offs in the Physical Design of On-chip Segmented Bus Architecture
  J. Guo, A. Papanikolaou, P. Marchal, F. Catthoor (IMEC v.z.w., Belgium)

DINNER ON YOUR OWN
SUNDAY

Session 6: Physical Interconnect Analysis and Optimization (9:00 - 10:30) (Chair: Jens Lienig)

- **Impact of Interconnect Resistance Increase on System Performance of Low Power and High Performance Designs**
  M. Bamal (IMEC, Katholieke Universiteit Leuven, Belgium), Y. Travaly (IMEC, Belgium), W. Zhang (IMEC, Katholieke Universiteit Leuven, Belgium), M. Stucchi (IMEC, Belgium), K. Maex (IMEC, Katholieke Universiteit Leuven, Belgium)

- **Statistical Crosstalk Aggressor Alignment Aware Interconnect Delay Calculation**
  A. B. Kahng, B. Liu, X. Xu (University of California at San Diego, USA)

- **Constant Impedance Scaling Paradigm for Interconnect Synthesis**
  J. Balachandran, S. Brebels, G. Carchon (IMEC vzw, Belgium), M. Kuijk (Vrije Universiteit Brussel, Belgium), W. De Raedt (IMEC vzw, Belgium), B. Nauwelaers (Katholieke Universiteit Leuven, Belgium), E. Beyne (IMEC vzw, Belgium)

BREAK (10:30 - 11:00)

Session 7: Optimal Interconnect Buffering (11:00 - 12:30) (Chair: Igor Markov)

- **The Scaling of Interconnect Buffer Needs (Invited Talk)**
  P. Saxena (Synopsys, Inc., USA)

- **Minimal-Power, Delay-Balanced Smart Repeaters for Interconnects in the Nanometer Regime**
  R. Weerasekera (KTH Information and Communication Technology, Sweden), D. Pamunuwa (Lancaster University, UK), L.-R. Zheng, H. Tenhunen (KTH Information and Communication Technology, Sweden)

LUNCH (12:30 - 14:00)

AFTERNOON SOCIAL EVENT:

Guided walking tour of downtown Munich (English speaking guide)
Start: Marienplatz at 14:30