CALL FOR PAPERS:

IEEE Transactions on VLSI Systems

Special section on System Level Interconnect Prediction

Submission Deadline: July 1st, 2006
Target Publication Date: Jan.-March 2007

Interconnect properties have become increasingly important for overall system performance and yield. Early evaluation and estimation of interconnect properties on all levels of design are crucial for fast design convergence. This Special Section aims at providing a view on the latest developments in system level interconnect prediction techniques. Papers that build on results published in the last System Level Interconnect Prediction Workshop (SLIP 2006) are especially welcomed but new submissions are more than welcome as well.

Topics of interest include, but are not limited to

- **Interconnect prediction methodology:** statistical properties of complex interconnect systems, techniques and calibrations for interconnect estimation, estimation of interconnect design parameters
- **Applications in system design:** interconnect parameter and yield estimation for use in architecture design and EDA, interconnect planning for specific objectives or target technologies
- **Applications in technology evaluation:** interconnect technology prediction for roadmap projections, evaluation of interconnect technologies in a system's context, architectural effects of interconnect optimization

Authors are encouraged to submit original, high-quality research contributions that will not require major revisions.

The Guest Editors for this Special Issue are:

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Submission instructions:

Manuscripts are subject to peer review and should be submitted online through IEEE Manuscript Central at http://tvlsi-ieee.manuscriptcentral.com by **July 1st**. During the Manuscript Central login, when prompted for MANUSCRIPT TYPE, be sure to indicate that your submission is for a SPECIAL SECTION. Also, you will be prompted for additional comments to the editor-in-chief. Please include the following comment at this stage and also on the title page of your actual manuscript:

SPECIAL SECTION ON SYSTEM LEVEL INTERCONNECT PREDICTION -- GUEST EDITORS JONI DAMBRE AND MIKE HUTTON

Regular paper submissions should be 8-10 pages in length and brief papers should be 3-4 pages in length. Please follow the submission guidelines specified by the IEEE Transactions on VLSI Systems.