Energy/area/delay trade-offs in the physical design of on-chip segmented bus architecture

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OUTLINE

Introduction

Optimization targets at floorplanning stage

Exploration methodology

Experiments

Conclusions

Energy is very important for embedded systems

The embedded systems are driven by the portable batteries, which are power and energy limited

Customers are willing to pay a bit more for devices with longer battery life times

Physical design must be linked to system level design for global optimization

Embedded systems

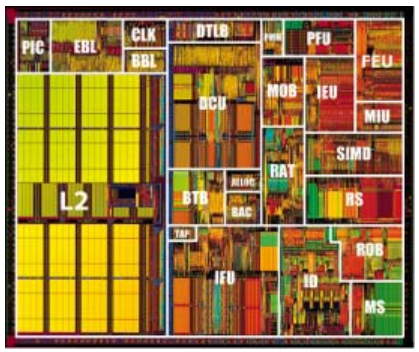
System-level design

Physical design

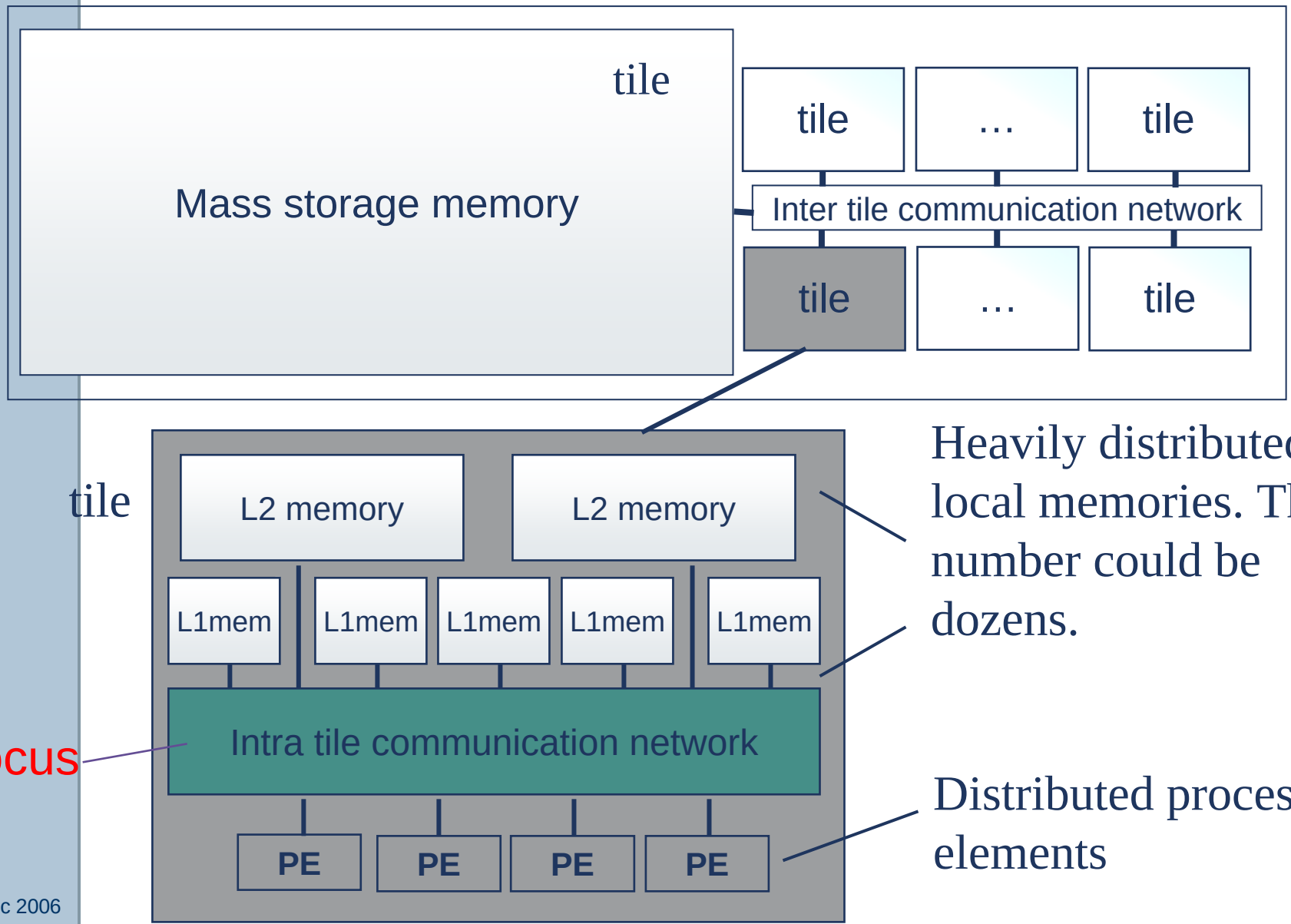
Links between different design phases

Data transfer activity information

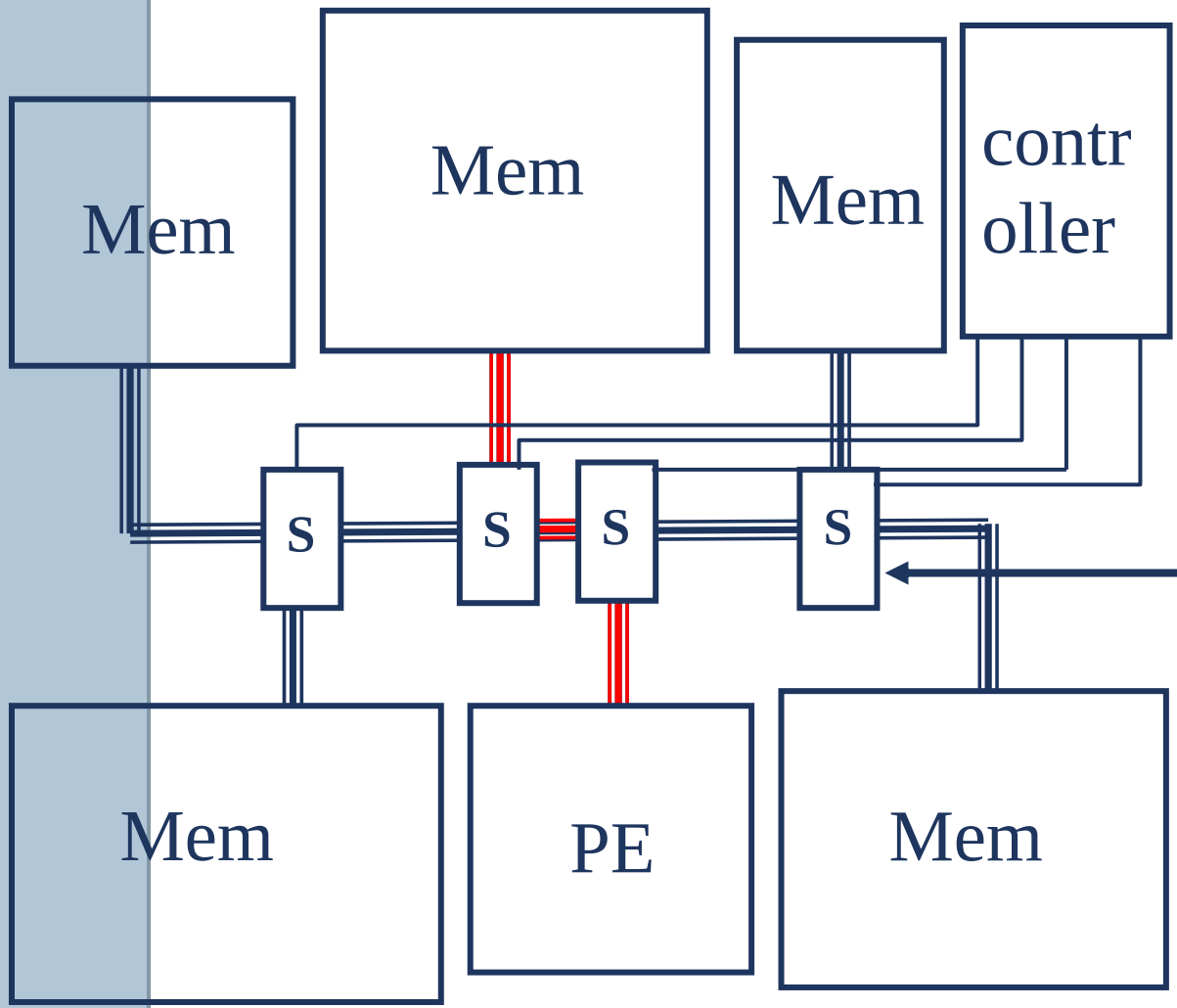
Geometry information

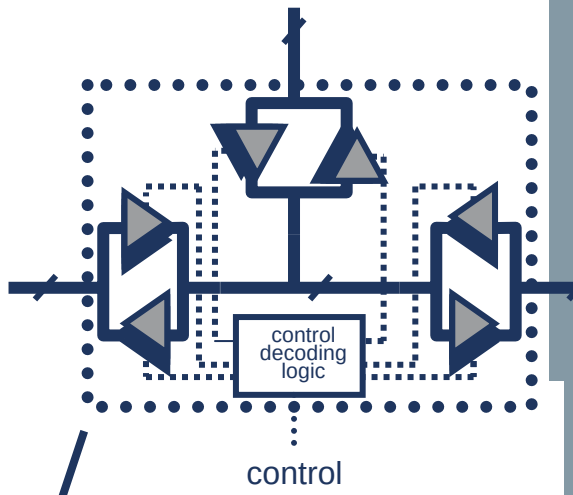


We focus on the intra-tile communication networks



On-chip segmented bus architecture based on shared bus



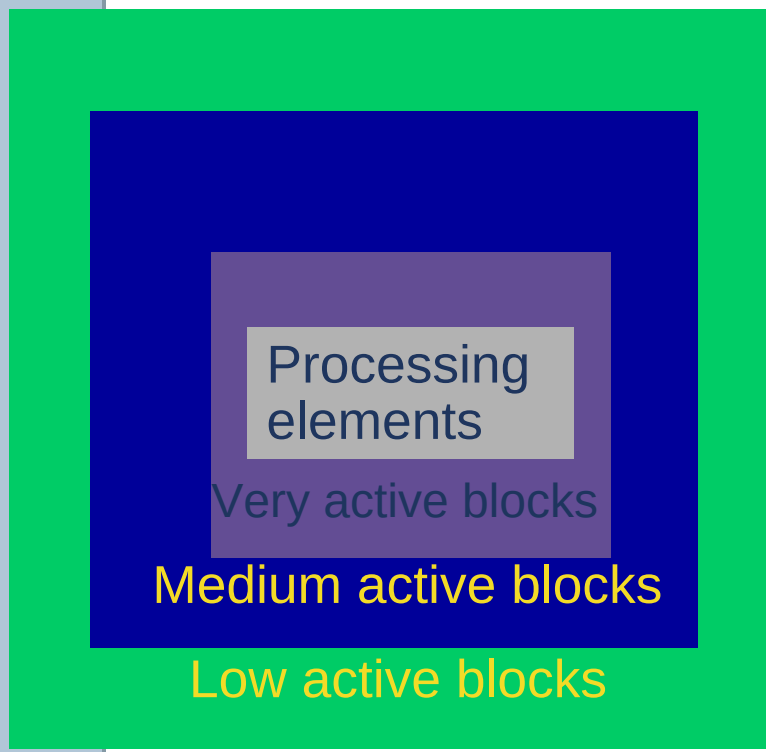


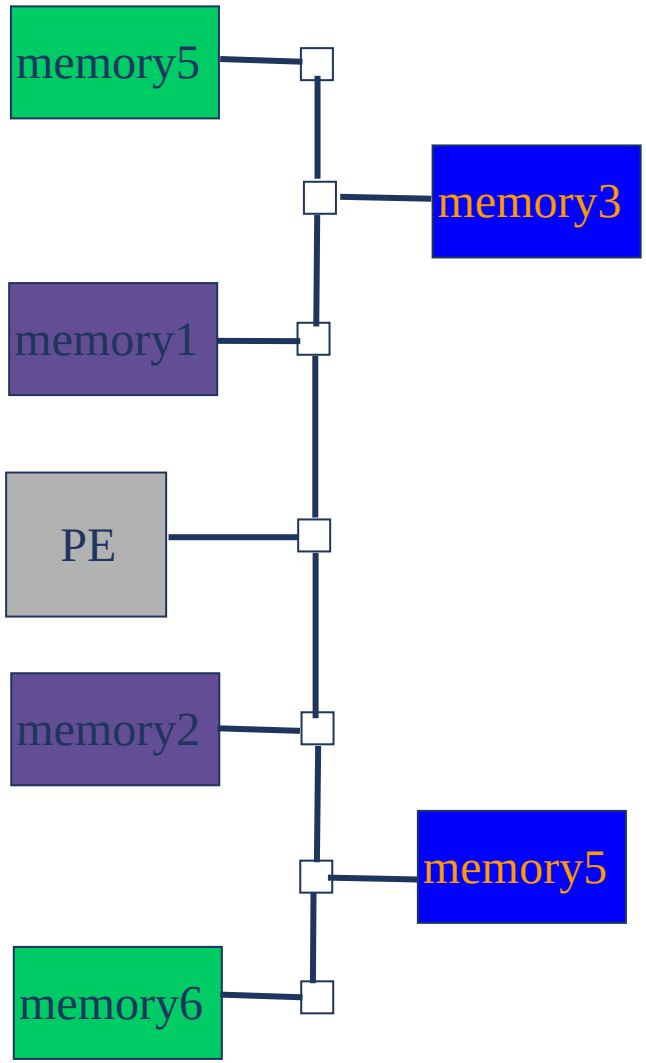
Switches

Shared bus architecture

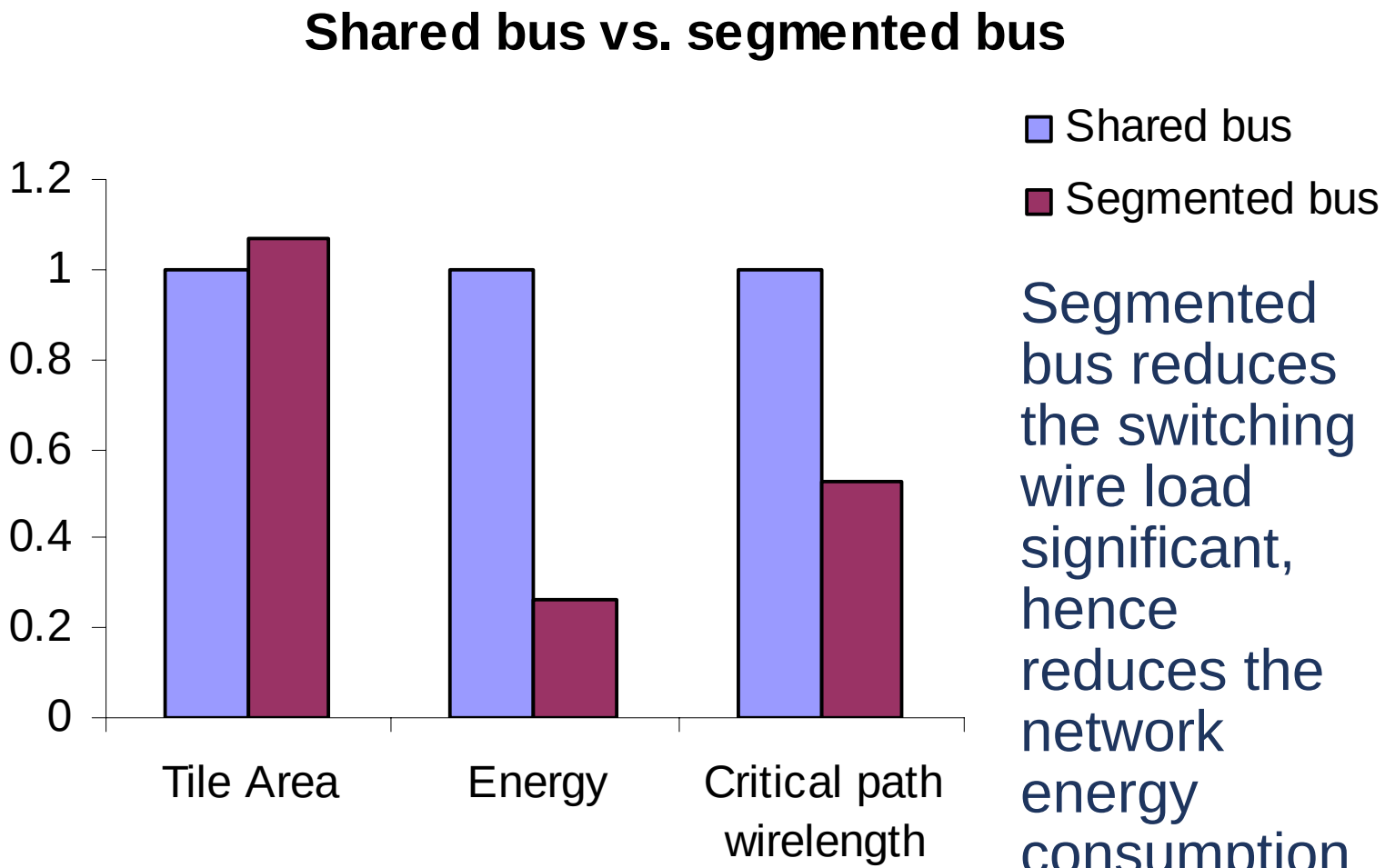
System level decision: activity-aware netlist for energy optimal solutions

Blocks that communicate very frequently should be ordered close to each other and vice versa



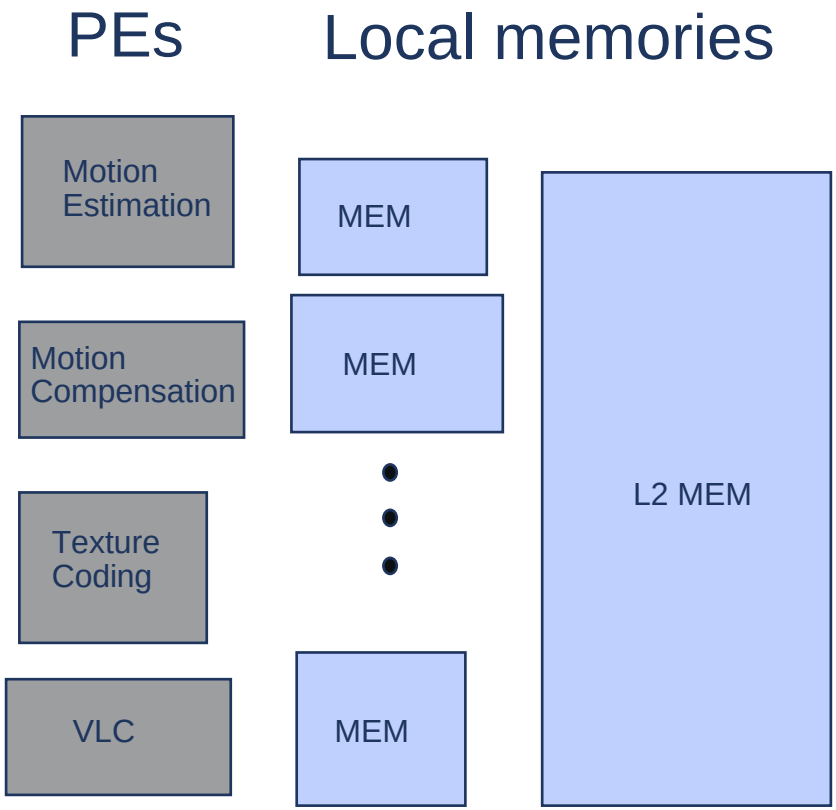


segmented bus vs. shared bus, MPEG4 encoder driver



Segmented bus reduces the switching wire load significant, hence reduces the network energy consumption and the critical path delay

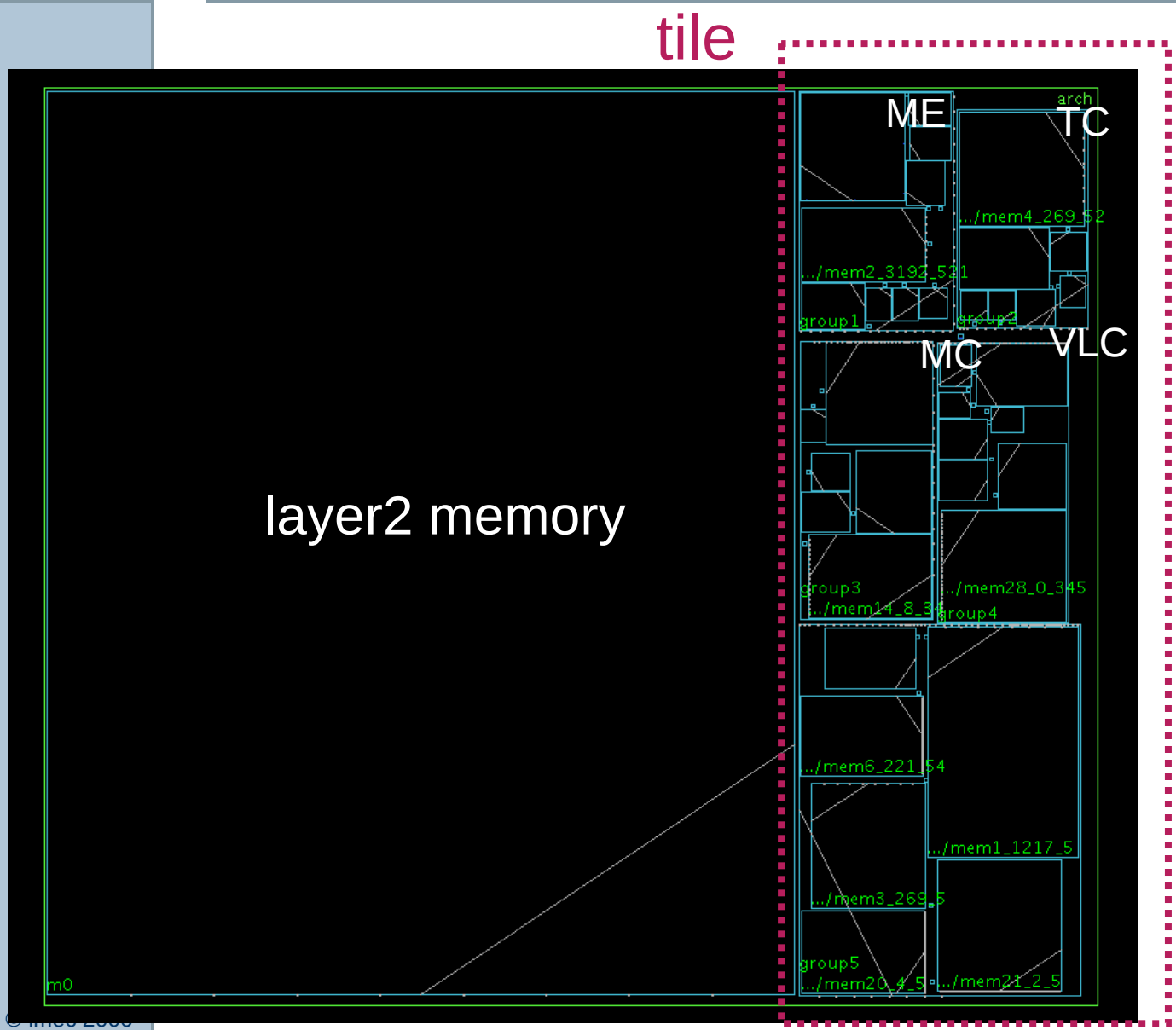
Hard macro block based floorplanning



MPEG4 encoder

- The floorplanning is at block level-> IP reuse
- Size & shape of the macro block are fixed -> avoid overruling the already made decisions at higher level. Changing the shape of an IP blocks alters its energy consumption per operation

Floorplan result demonstrated on MPEG4 encoder



Large layer2 memory dominates the chip area.

Some area overhead in the small tile has slight impact on the total chip area, but improves network energy significantly

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Physical design level: Tradeoffs for various criteria

Area

- Directly related to the manufacture cost
- Would like to pack all the modules very tightly

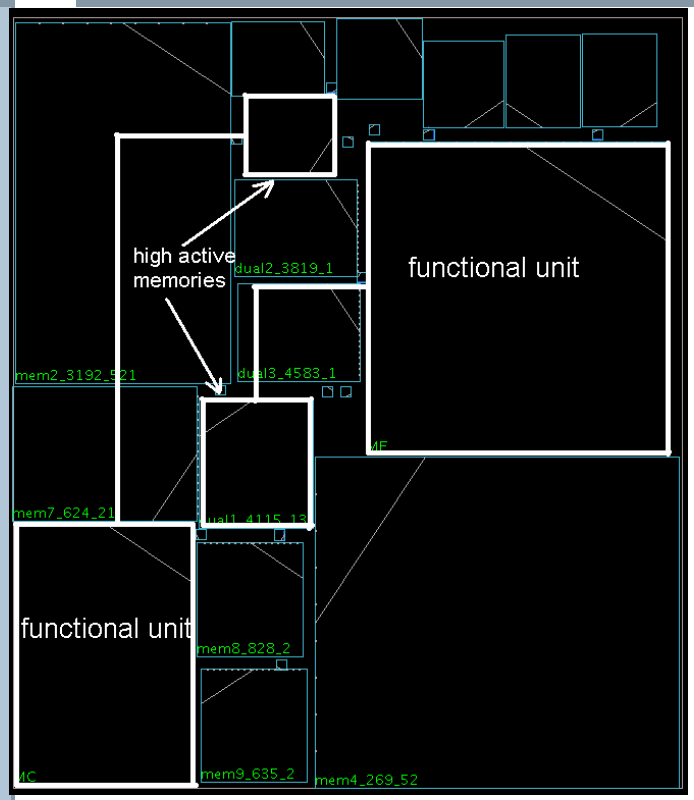
Energy dissipation (communication network)

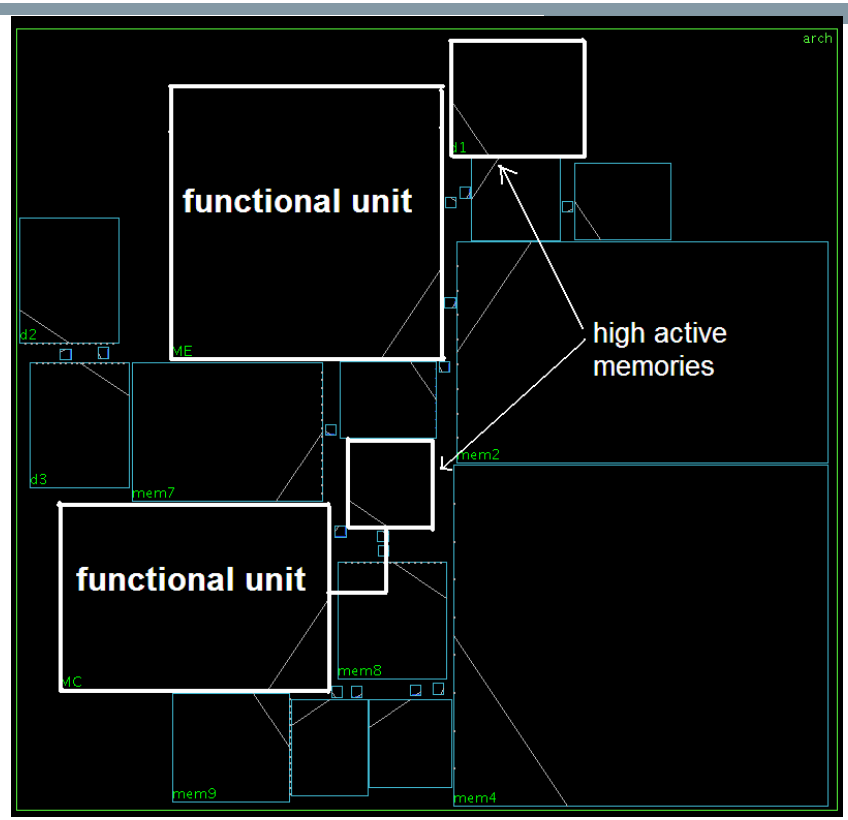
- With technology nodes shrinking down, interconnects consume considerable energy
- A well designed layout helps to reduce network energy consumption

Timing closure

- Data need to be transferred to the destinations in the designed time budget

Example of tradeoffs between chip area and network energy (MPEG4 application)





Area: 5.108 mm2
energy: 2.766*(1e-4) J

Area optimal layout

Area: 7.832 mm2
energy: 0.790*(1e-4) J

Network energy optimal layout

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Physical design tools used in our experiments

Floorplanning tool (Parquet)

-- Academic placer, developed by Univ. of Michigan

-- Macro block based floorplanner

Routing tool : Magma

-- Commercial physical design tool

-- Not supporting the automated floorplanning for macro blocks

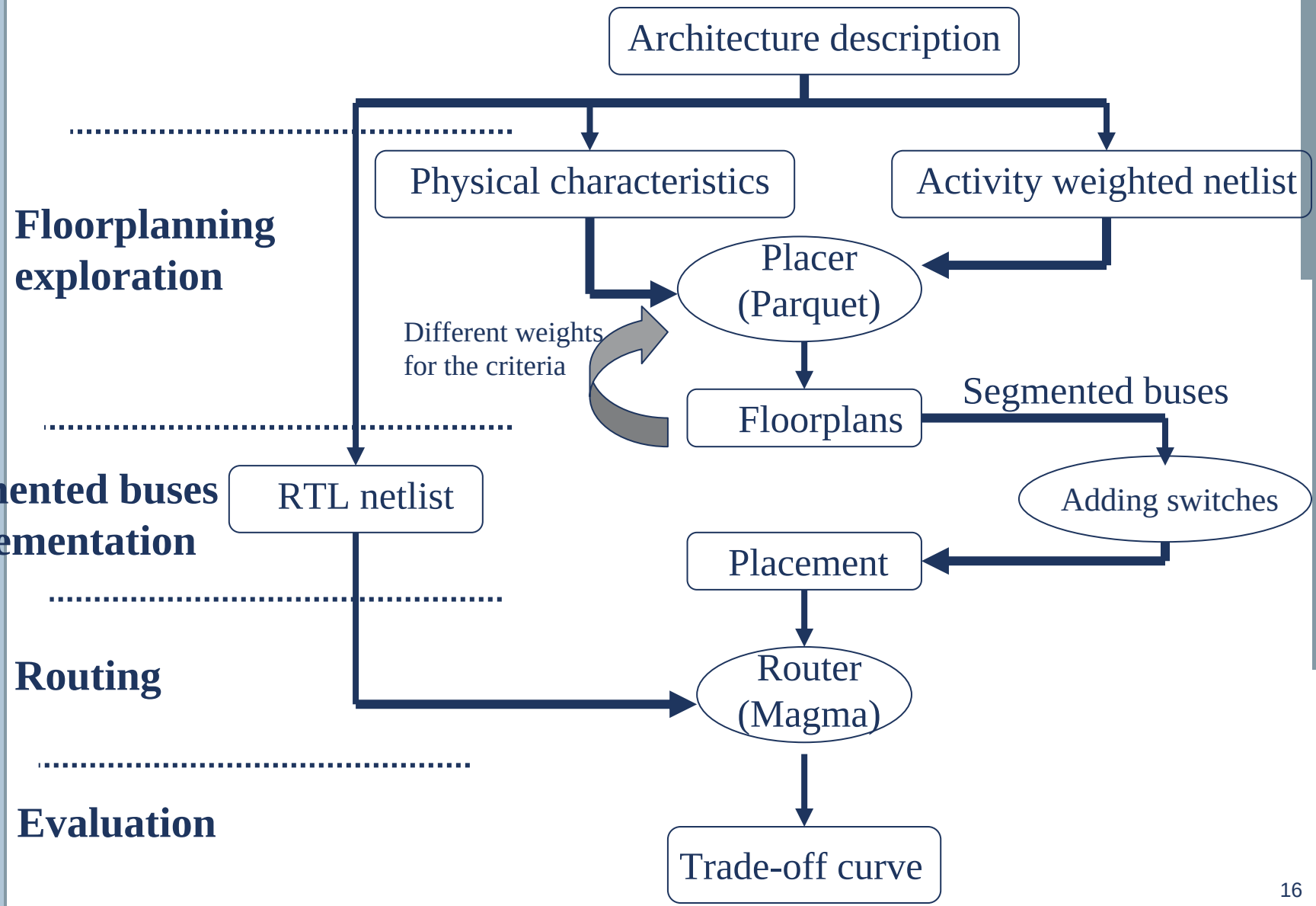
-- Detailed routing, layout evaluation

Additional scripts

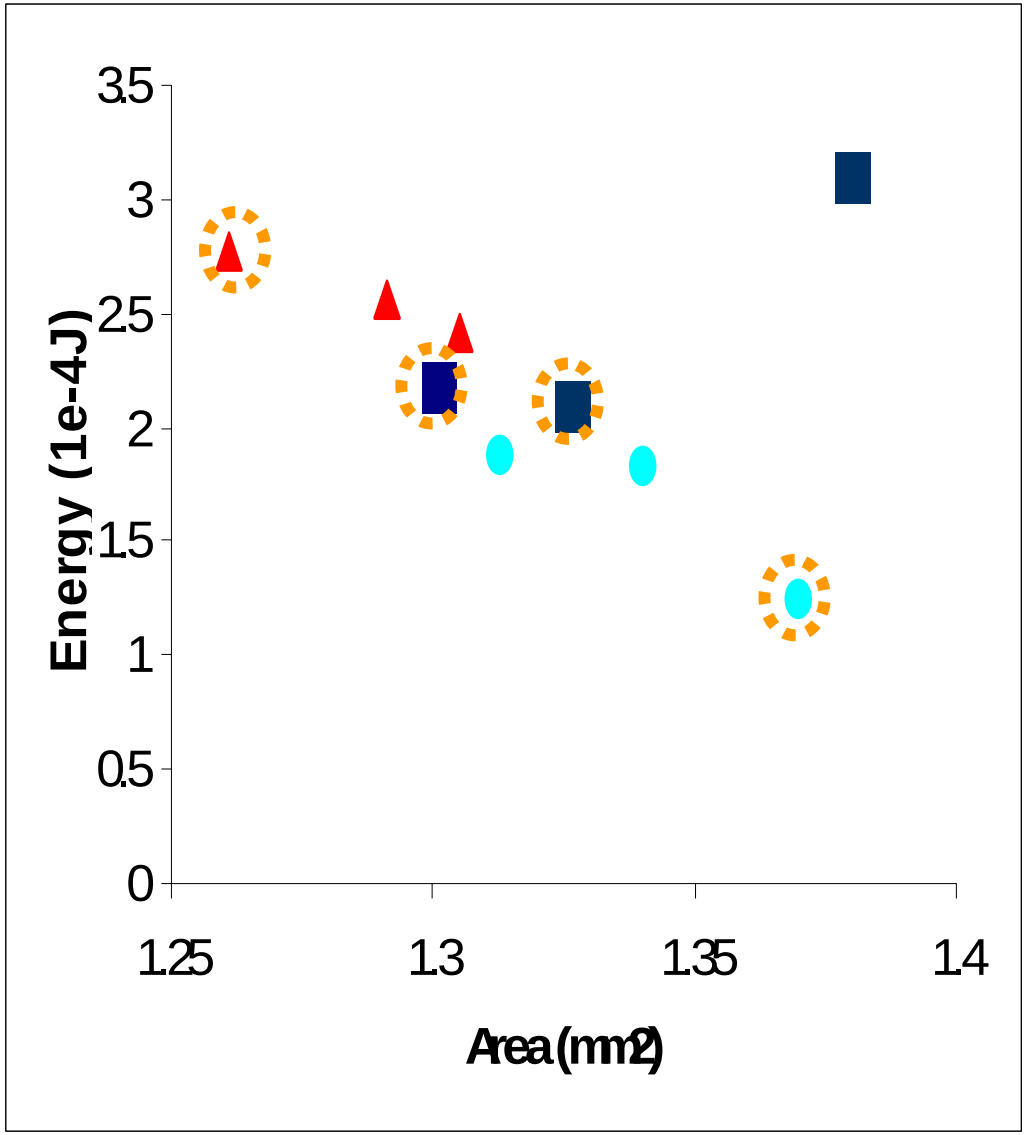
-- Switches insertion

-- Converting Parquet output files into MAGMA input files

Trade-offs exploration methodology flow-graph



The impact of the different weight setting on the chip area and network energy

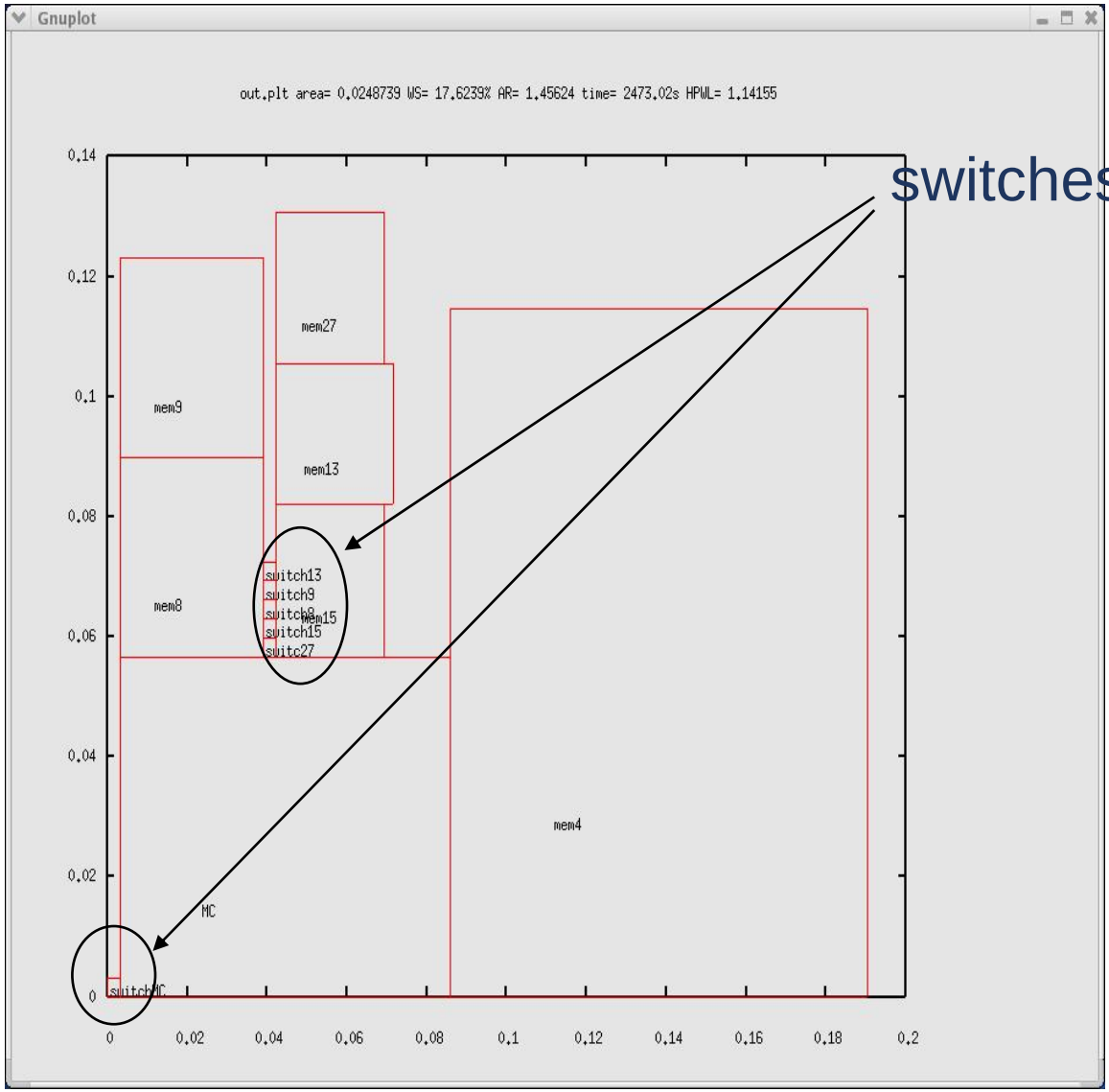


We set different weights for different criteria in Parquet (academic placer)

- area weight =1, activity weight =0
- area weight =0.5, activity weight =0.5
- area weight =0, activity weight =1

The weight for each criterion decides the values of this criterion after floorplanning stage

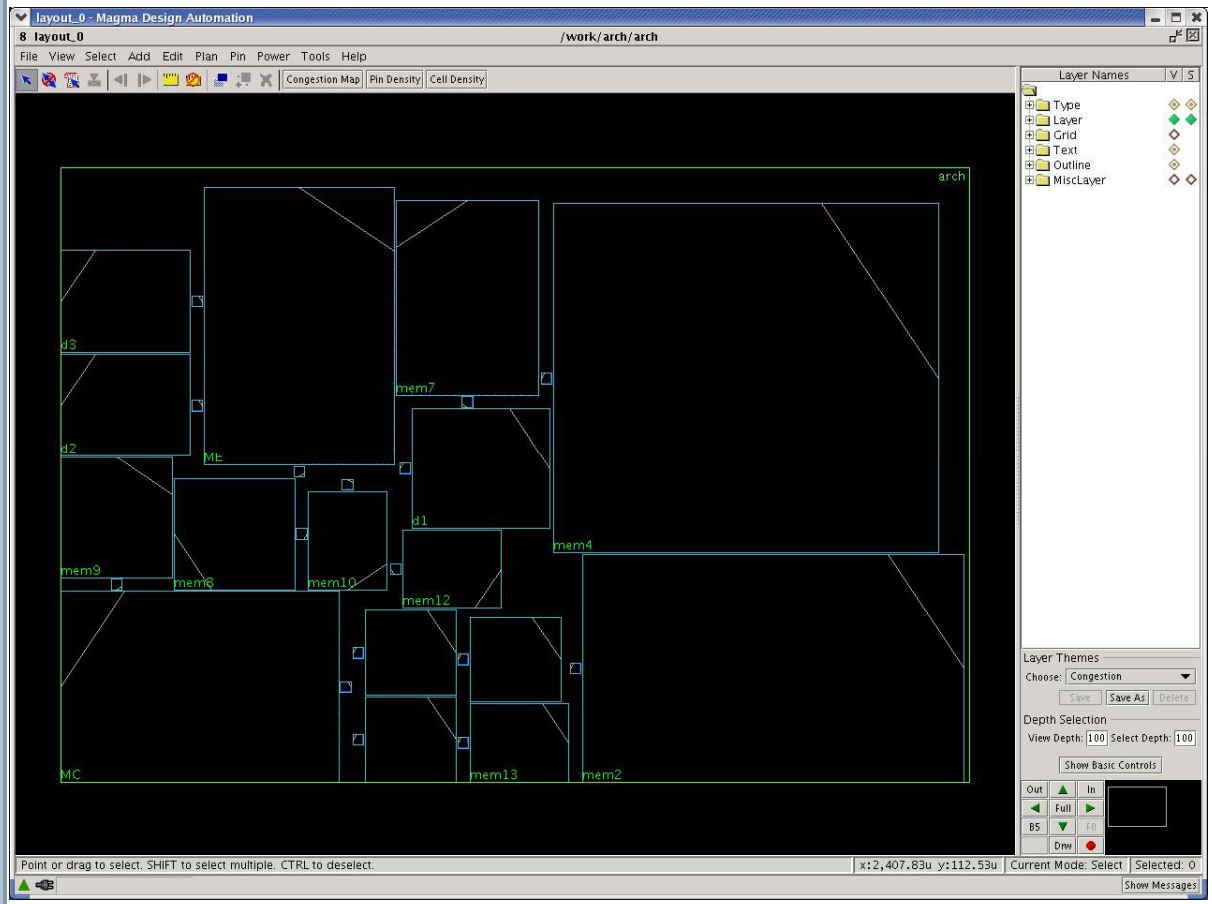
Why do we insert the switches after floorplanning?



switches

When the size of the switches is much smaller than the size of the memories, Parquet can not place the switches in appropriate locations.

Solution: add the switches after floorplanning



Step1: Parquet generates floorplan without switches

Step2: switches are added and imported to MAGMA:

- Close to the communication ports
- Without overlapping to all the other blocks

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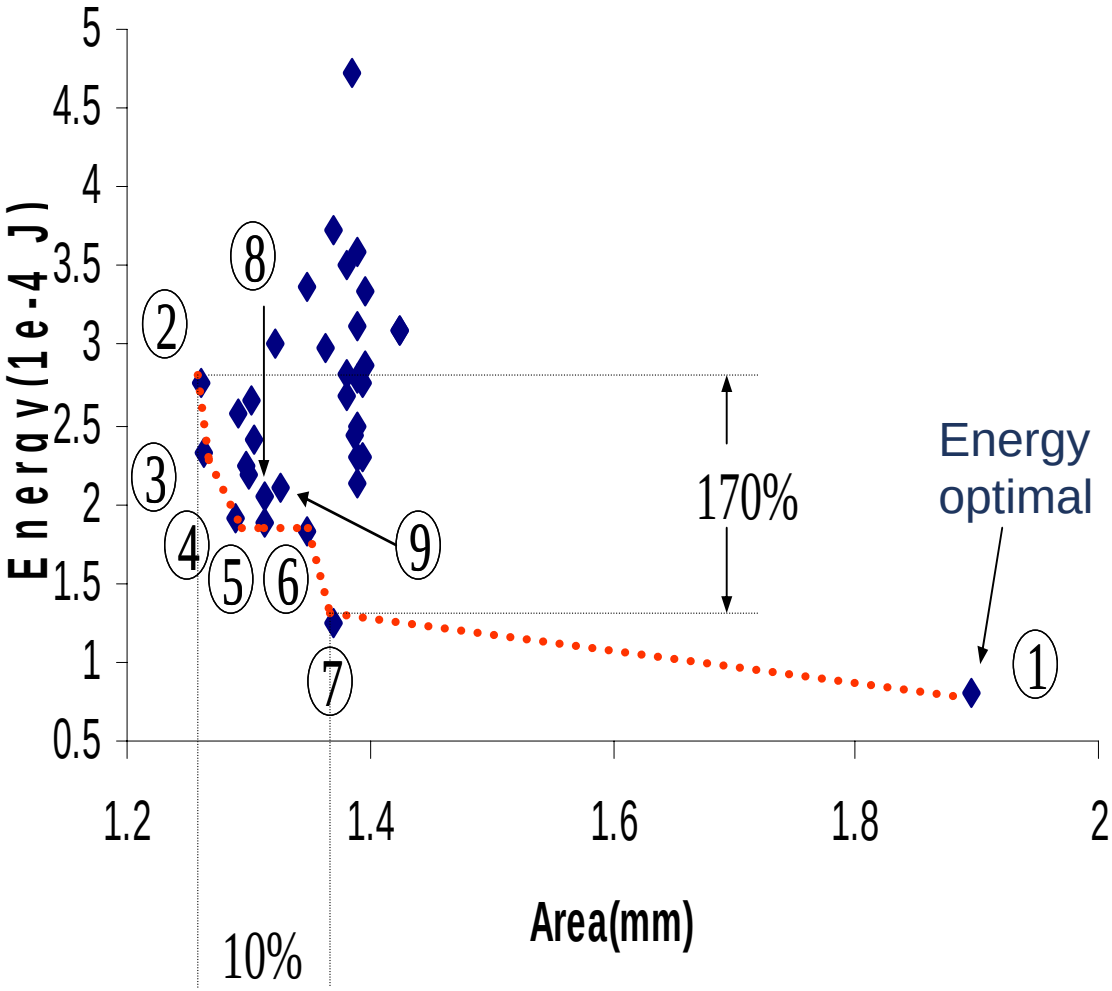
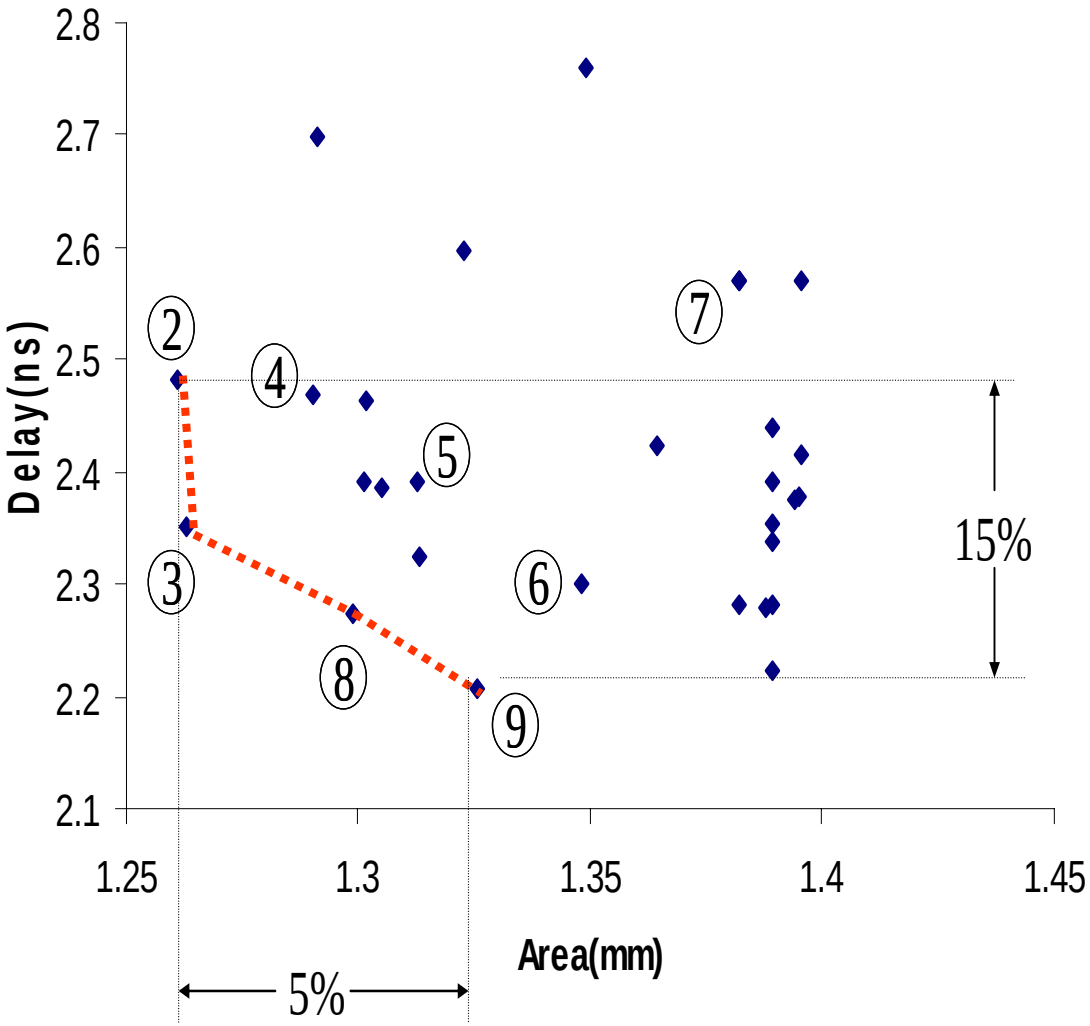
Area/Energy Pareto curve for MPEG4 encoder



With only 10% area overhead in the tile, we reduce energy consumption by a factor of 2.7

There are some intermediate tradeoff solutions for the designer to choose

Area/Delay Pareto curve for MPEG4 encoder



With 5% area variation, we can have 15% gain in delay

Efficient energy/delay/area decisions have to made in the three dimensional space to meet the specific design requirements

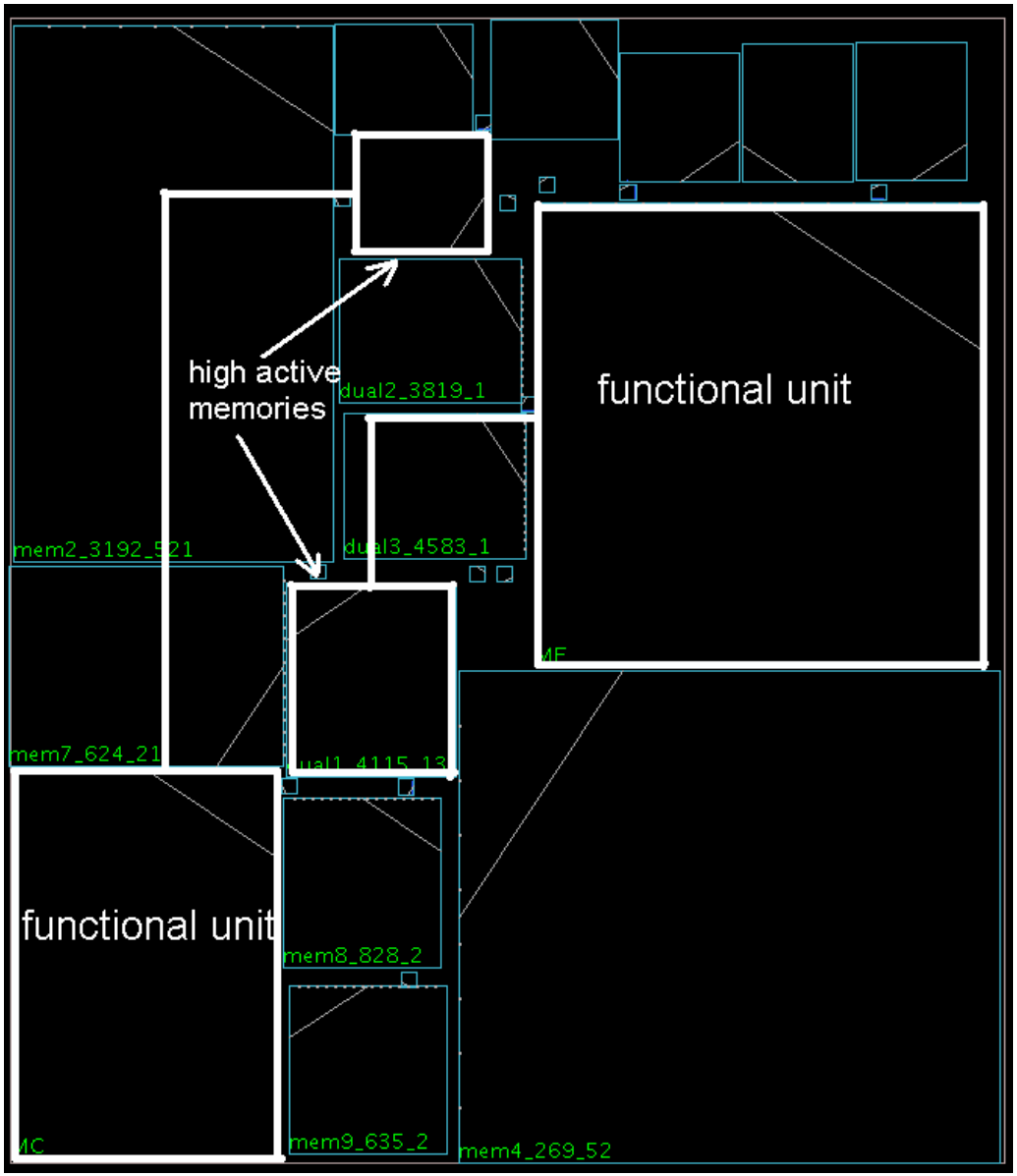
Conclusions

- Using the segmented bus, we can significantly improve network energy consumption compared to shared bus

- A design flow is introduced to explore the tradeoffs in network energy dissipation, chip area and delay efficiently

- A designer can significantly improve energy consumption with a slight penalty in area at physical design stage

Area optimal layout (MPEG4 application)



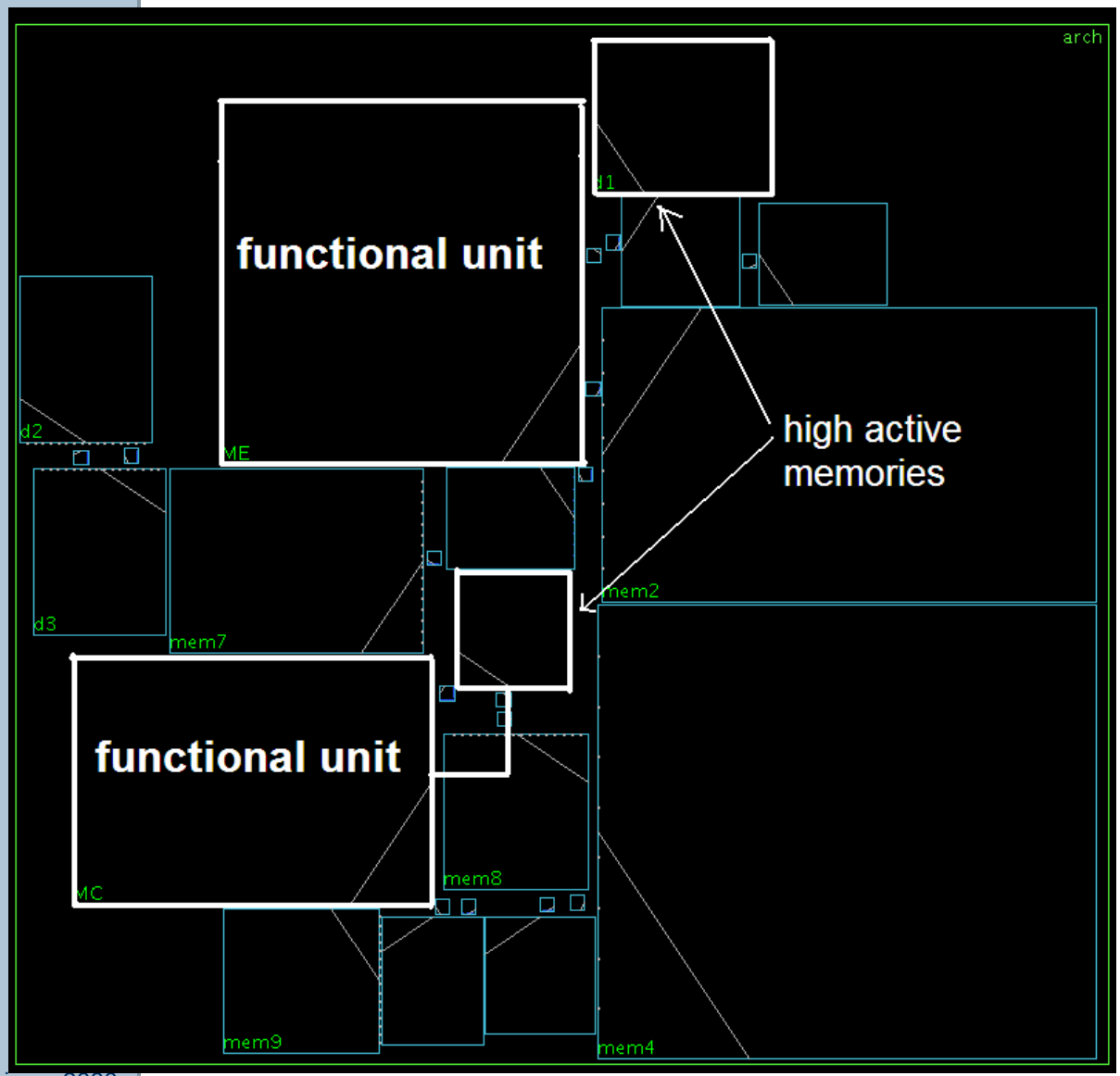
Area: 5.108 mm2

energy: 2.766*(1e-4)

The chip area utilization is high

The high active memories have long communication path, which cause large energy consumption

Communication energy optimal layout (MPEG4 application)



Area: 7.832 mm2

energy: 0.790*(1e-4)

The high active memories are placed very close to the functional unit, which benefits the network energy.

The layout is not quite compact