The Impact of Interstratal Interconnect Density on the Performance of Three-Dimensional Integrated Circuits

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Outline

• Introduction
• Method for system-level performance evaluation
• Wire-length distributions
• Results
  • System-level performances of 2D, ideal, semi-ideal and realistic 3D-ICs
  • Recently published data + benchmarking
• Conclusions
Introduction

• Signal delay, high power consumption are the problems associated with long, thin, dense interconnects

• Solutions under investigation
  • Optical interconnect, carbon nanotubes…
  • 3D-IC
Interconnection issues in 3D-IC  

#1

High-aspect-ratio through-wafer vias

Misalignment between device layers
Interconnection issues in 3D-IC #2

Example of state-of-the-art die-to-die via dimensions

- Via diameter: ~5µm
- Via height: ~50µm
- Via pitch: ~10µm

45-nm CMOS cell size: ~1.5µm x 1.5µm

Vertical routing in a 3D-IC at 45-nm node is limited

What are the consequences on 3D-IC performance
Method for system-level performance evaluation

- 45-nm CMOS compact model
- 100 ivx1x critical path
- Delay, dynamic switching energy
- 1000 trials

- 45-nm interconnect compact model
- 3D Wire length distributions
Example of a wire-length distribution

902,500 gates
CMOS045
5 metal levels
2D wire-length distribution – Davis model

\[ f_{2D}(l) = \Gamma M_{2D}(l) I_{2D}(l) \]

- Number of gate pairs separated by distance \( l \)
- Expected number of interconnects between two gates

\( l = 13 \) gate pitch

Block A – \( N_{A2D} \) gates
Block B – \( N_{B2D} \) gates
Block C – \( N_{C2D} \) gates

3D wire-length distribution – Rahman model

Stratum 1

Stratum 2

Stratum 3

Block A – N_{A3D} gates
Block B – N_{B3D} gates
Block C – N_{C3D} gates

3D wire-length distribution – Rahman model

Average values for $N_A, B, C$

$$N_{A3D} = 1$$

$$N_{B3D}(l) \approx \frac{1}{S} \left[ N_{B2D}(l) + 2N_{B2D}(l-t_S)u(l-t_S) + \ldots + 2N_{B2D}(l-(S-1)t_S)u(l-(S-1)t_S) + \ldots \right]$$

$$N_{C3D}(l) \approx \frac{1}{S} \left[ N_{C2D}(l) + 2N_{C2D}(l-t_S)u(l-t_S) + \ldots + 2N_{C2D}(l-(S-1)t_S)u(l-(S-1)t_S) + \ldots \right]$$

Observations

Observation 1: Transformation of Rahman model

\[ N_{B3D}(l) = N_{B2D}(l) + \frac{1}{S} \sum_{i=1}^{S-1} \left[ 2(S-i)N_{B2D}(l-it_s)u(l-it_s) \right] \]

\[ N_{C3D}(l) = N_{C2D}(l) + \frac{1}{S} \sum_{i=1}^{S-1} \left[ 2(S-i)N_{C2D}(l-it_s)u(l-it_s) \right] \]

Observation 2: In reality

Limited number of interstratal interconnects

Contribution of the 3\textsuperscript{rd} dimension will be much less

Concept of probability of connection to other strata
Observation 2: Example

<table>
<thead>
<tr>
<th></th>
<th>Stratum 1</th>
<th>Stratum 2</th>
<th>Stratum 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ideal</strong></td>
<td><img src="image1" alt="Ideal Grid" /></td>
<td><img src="image2" alt="Ideal Grid" /></td>
<td><img src="image3" alt="Ideal Grid" /></td>
</tr>
<tr>
<td><strong>Reality</strong> (limited number of interstratal interconnects)</td>
<td><img src="image4" alt="Reality Grid" /></td>
<td><img src="image5" alt="Reality Grid" /></td>
<td><img src="image6" alt="Reality Grid" /></td>
</tr>
</tbody>
</table>
3D wire-length distribution – New model

\[ N_{A3D} = 1 \]

\[ N_{B3D}(l) = N_{B2D}(l) + \frac{1}{S} \sum_{i=1}^{S-1} \left[ 2(S-i)N_{B2D}(l-it_s)u(l-it_s)P_{\text{density}}^i \right] \]

\[ N_{C3D}(l) = N_{C2D}(l) + \frac{1}{S} \sum_{i=1}^{S-1} \left[ 2(S-i)N_{C2D}(l-it_s)u(l-it_s)P_{\text{density}}^i \right] \]

Examples

\[ P_{\text{density}} = 1 \] --- Ideal case, back to Rahman model
\[ P_{\text{density}} = 0.5 \] --- Semi-ideal case
\[ P_{\text{density}} = 0.1 \] --- Realistic case

CMOS045 dimensions \( \rightarrow \) Interstratal interconnect pitch

\[ P_{\text{density}} = 1 \] --- Pitch \~ 1.5 µm
\[ P_{\text{density}} = 0.5 \] --- Pitch \~ 3 µm
\[ P_{\text{density}} = 0.1 \] --- Pitch \~ 15µm
Wire-length distributions of 2D, ideal, semi-ideal and realistic 3D-ICs

- 3,500,000 gates
- $p = 0.66$, $\alpha_k = 3$
- $t_S = 1$ gate pitch
- 2 strata (3D)
- CMOS045

Zoom in

Number of wires vs Length (gate pitch)

- 3D – Ideal - Red
  - $P = 1$
- 3D – Semi ideal - Dotted Magenta
  - $P = 0.5$
- 3D – Realistic - Black
  - $P = 0.1$
- 2D – Blue

Decreasing number of short length interconnects
Increasing number of medium length interconnects
Method for system-level performance evaluation

- 45-nm CMOS compact model
- 45-nm interconnect compact model
- 3D Wire length distributions

- 100 ivx1x critical path
- Delay, dynamic switching energy
- 1000 trials

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Results

1. Delay versus architectures

- Ideal 3D interconnect architecture only shows a modest performance improvement (approx. 10%)
- Realistic 3D interconnect architecture does not improve performance
- Increase number of strata does not significantly improve performance

2. Dynamic switching energy versus architectures

Recently proposed dimensions & properties for 45-nm CMOS
Recently published data on 3D-IC
Performance of 3D iA32 microprocessor

2D floor plan of a deeply pipelined iA32 core
3D floor plan of a deeply pipelined iA32 core

Recent published data on 3D-IC

Performance of 3D iA32 microprocessor

Required die-to-die via pitch (μm) density in 90nm process

Performance improvement

Speed: 15%
Power: 15%

## Benchmarking

<table>
<thead>
<tr>
<th></th>
<th>Our analysis</th>
<th>Published data</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology node</strong></td>
<td>45-nm</td>
<td>90-nm</td>
</tr>
<tr>
<td><strong>Circuit type</strong></td>
<td>Random logic network</td>
<td>Deeply pipelined microprocessor</td>
</tr>
<tr>
<td><strong>Number of device layers</strong></td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>Via pitch density</strong></td>
<td>1.5-µm; 3-µm; 15-µm</td>
<td>Minimum: 9 µm</td>
</tr>
<tr>
<td><strong>Performance improvement</strong></td>
<td>1.5-µm via pitch: +10%</td>
<td>15%</td>
</tr>
<tr>
<td></td>
<td>3-µm via pitch: -0%</td>
<td></td>
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<tr>
<td></td>
<td>15-µm via pitch: -15%</td>
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Conclusions

• Interstratal interconnect density plays a crucial role in determining the performance of 3D random logic networks

• It is indicated that serious efforts need to be spent on realizing high density interstratal interconnect for CMOS045 and smaller nodes in order to benefit from 3D architecture

• Increasing the number of strata does not significantly increase the performance of a 3D-IC
Acknowledgement

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  • Manish Garg
  • Laurent Le Cam
  • Gerben Doornbos
  • Ranick Ng
3D wire-length distributions

(a) Graph showing the relationship between the number of wires and wire length (gate pitch) for Ideal 3D-IC with 2 strata and Conventional 2D-IC.
3D wire-length distributions

- Ideal 3D-IC with 2 strata (P density = 1)
- Semi-ideal 3D-IC with 2 strata (P density = 0.5)
- Realistic 3D-IC with 2 strata (P density = 0.1)

Number of wires vs. Wire length (gate pitch)
3D wire-length distributions

- Ideal 3D-IC with 2 strata (P density = 1)
- Semi-ideal 3D-IC with 2 strata (P density = 0.5)
- Realistic 3D-IC with 2 strata (P density = 0.1)