Prediction Model for Evaluation of Reconfigurable Interconnects in Distributed Shared-Memory Systems

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SLIP'05, April 2-3 2005, San Francisco



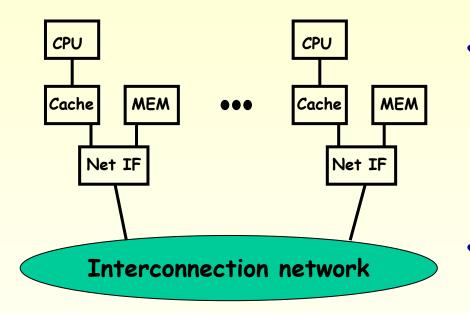
Outline

- Introduction
- Reconfigurable Optical Networks
- Prediction Model
- Results
- Future work & conclusions





Architecture of a distributed shared-memory system

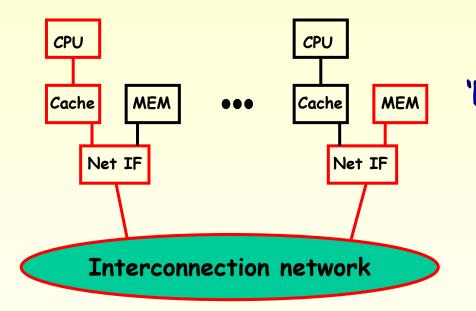


• Nodes:

- Processor
- Caches
- Main memory
- Network interface
- Interconnection network
 - Packet switched



Architecture of a distributed shared-memory system



'Remote' memory access: handled by the network interfaces, requires use of the interconnection network

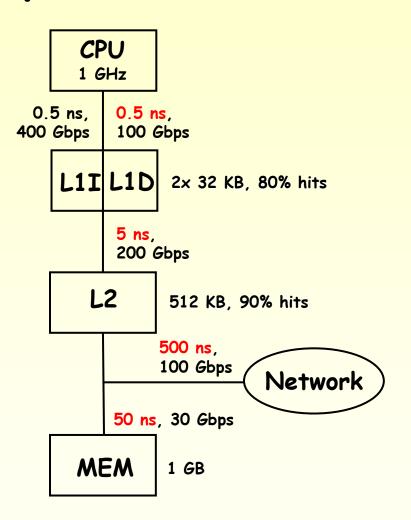


Interconnect requirements

 Network latency is a major bottleneck:

> instruction (.5 ns) << local memory access (50 ns)

<< remote memory access
(500 ns)</pre>



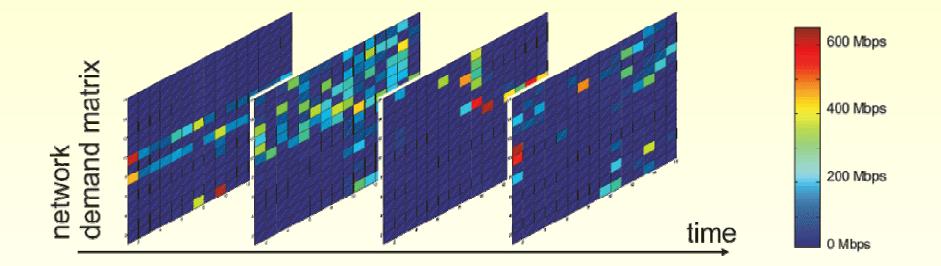
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Interconnect requirements

Non-uniform network traffic in space and time



=> Reconfigurable network?



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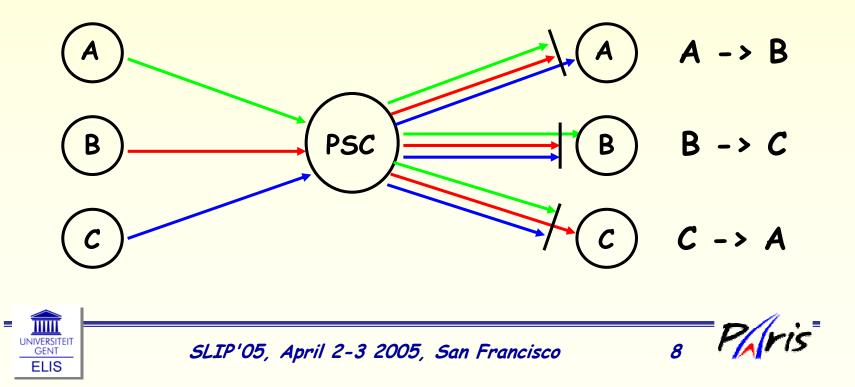
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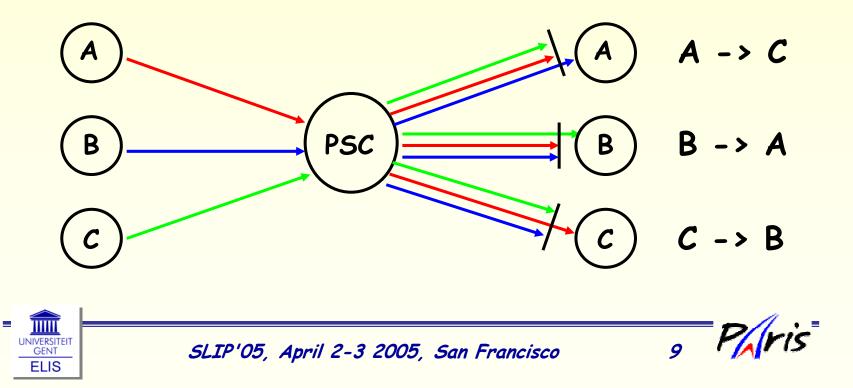
Reconfigurable Optical Networks

- WDM (wavelength division multiplexing)
 - Tunable lasers / detectors
 - Passive star coupler (PSC)



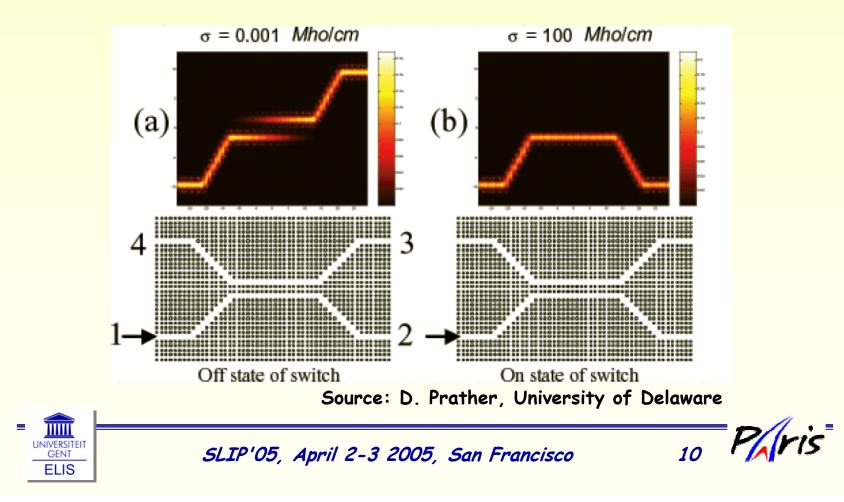
Reconfigurable Optical Networks

- WDM (wavelength division multiplexing)
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Reconfigurable Optical Networks

Photonic Crystal components (crossbar)



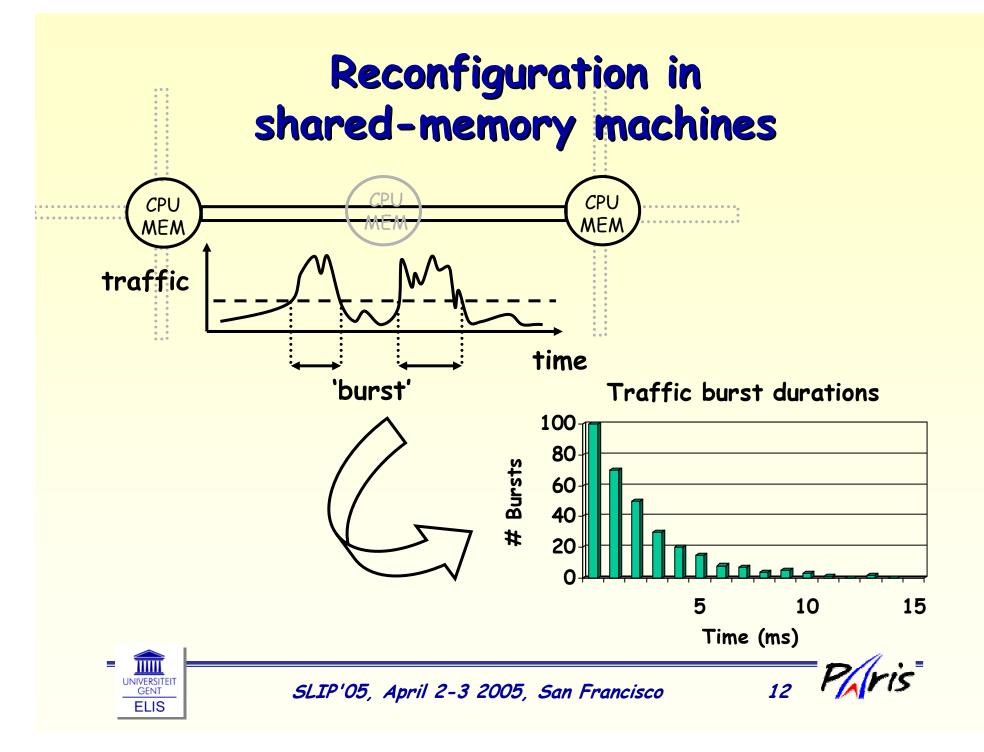
Reconfiguration in shared-memory machines

- Reconfiguration speed: up to 1 ms
- One memory access: < 1 μ s
- Locality needed in address streams!

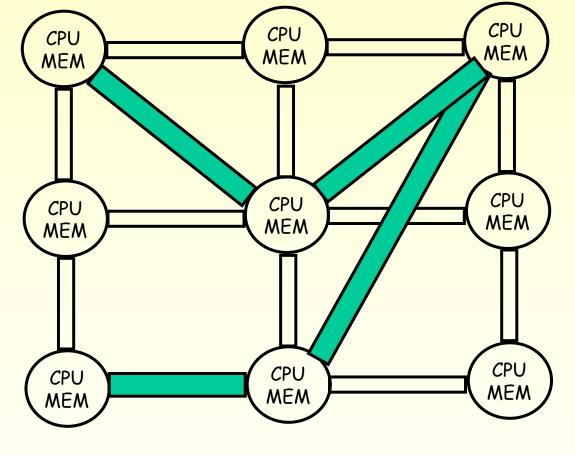
(Traffic Temporal Analysis for Reconfigurable Interconnects in Shared-Memory Systems, W. Heirman et. al., Reconfigurable Architectures Workshop, April 4-5, 2005, Denver, CO)

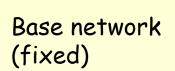






Reconfiguration in shared-memory machines

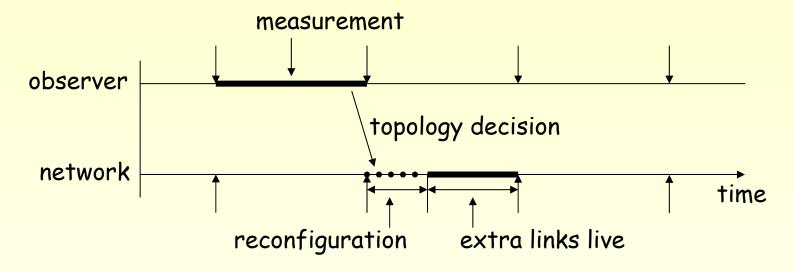




Extra links (reconfigurable)



Reconfiguration in shared-memory machines



 Requirement: Reconfiguration time « reconfiguration interval « burst duration



Evaluating network performance

- Full-system simulations are needed:
 - Current statistical traffic models don't exhibit the 'bursty behavior' exploited here
 - 'Application speedup' cannot be derived from network performance alone
- The simulation needs to model tens of processors, caches, and the interconnection network
- Different benchmarks





Evaluating network performance

Evaluating just one set of network parameters takes hours of simulations...

How can we do this faster?

Derive performance for several sets of network parameters from one simulation!



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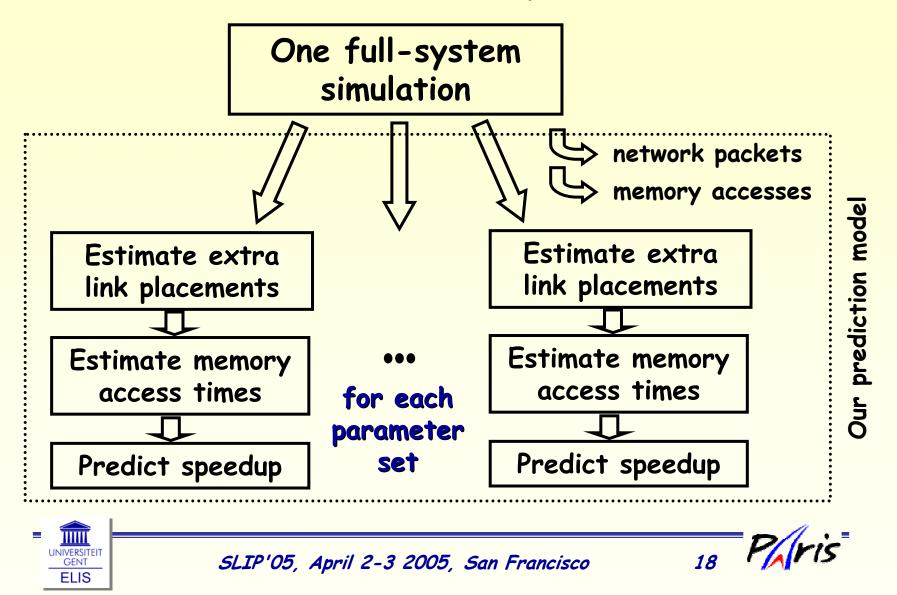


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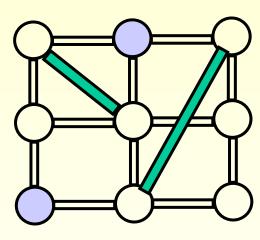
Estimate extra link placement: delta t = 1 n = 2 delta t = 2 n = 4 time

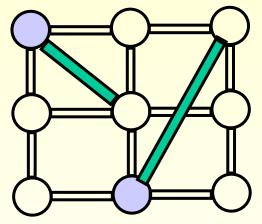
Parameters: reconfiguration interval (delta t), number of extra links (n), link placement algorithm

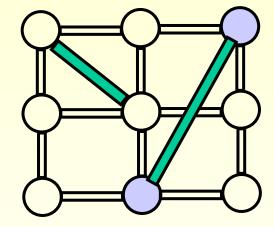


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• Estimate new memory access latency for each transaction:







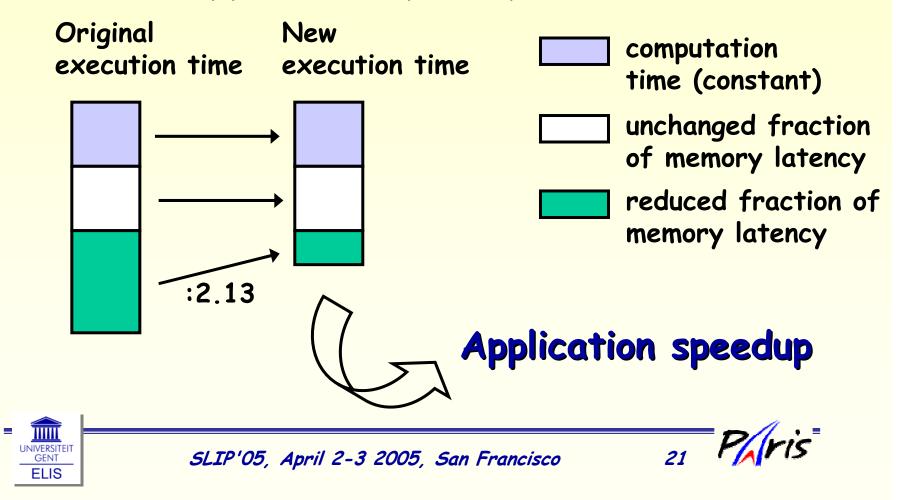
No change

No change(!)

Reduced access time



Predict application speedup:



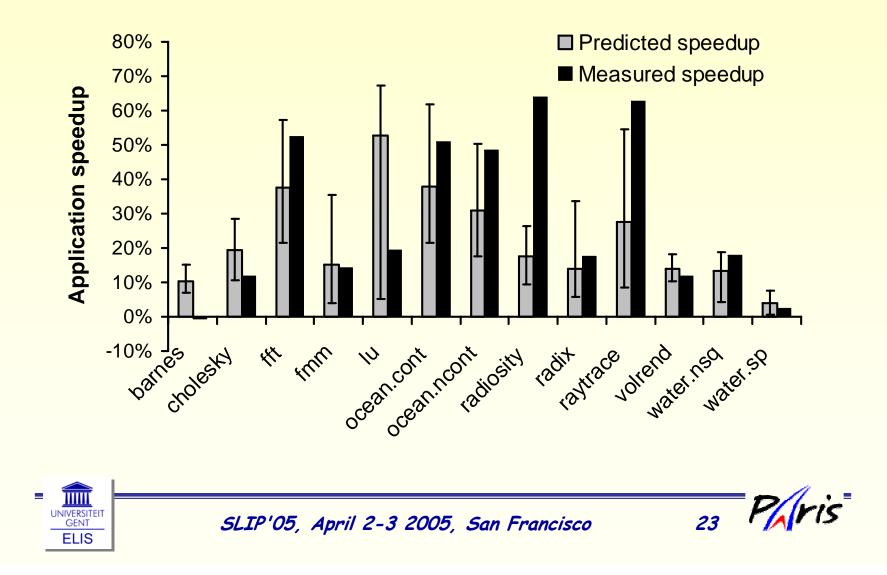
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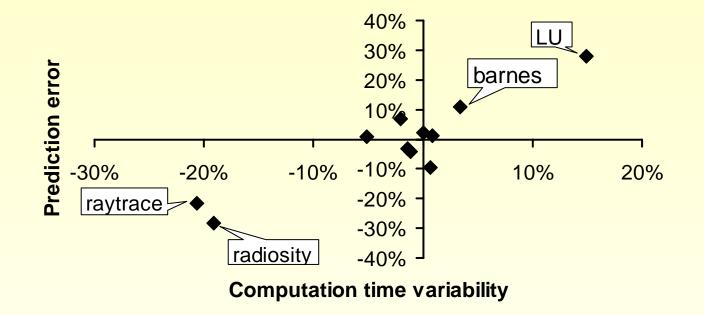
Assumptions

- Access latency is not hidden by out-of-order execution
- Average reduction factor is used for all improved memory accesses (2.13 for 4x4 torus network)
- Memory accesses require only 2 nodes
- Computation time remains constant
- Congestion is not modeled
- Any combination of extra links can be made
- Extra links are not used as part of a path





Results: application variability



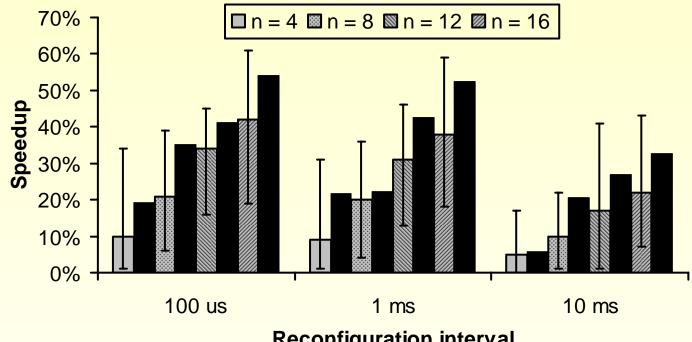
 Correlation between computation time variability and prediction error is high, this could explain larger errors in some benchmarks

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Results: different parameters



Reconfiguration interval

FFT benchmark, results for different reconfiguration intervals and # extra links: good relative prediction



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Future work

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Conclusions

- Using our technique, good predictions can be made using much less time-consuming simulations
- Good relative accuracy over a range of parameters allows for quick design-space exploration
- Further refinements can be made by including application variability and congestion



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