Self-Consistent Power/Performance/Reliability Analysis for Copper Interconnects

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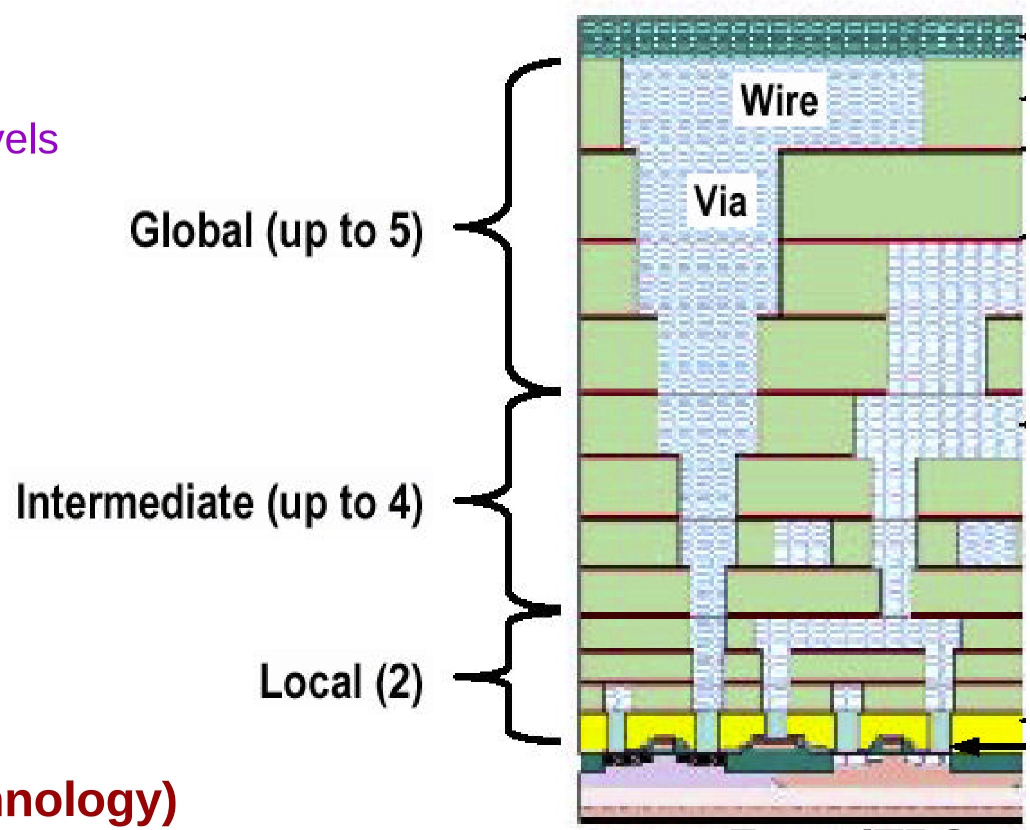
MARCO Interconnect Focus Center

Interconnect Scaling

- **Scaling Trends**
  - More wires
  - Shrinking and more metal levels
  - Resistance & Capacitance ↑
    ⇒ Performance deteriorates

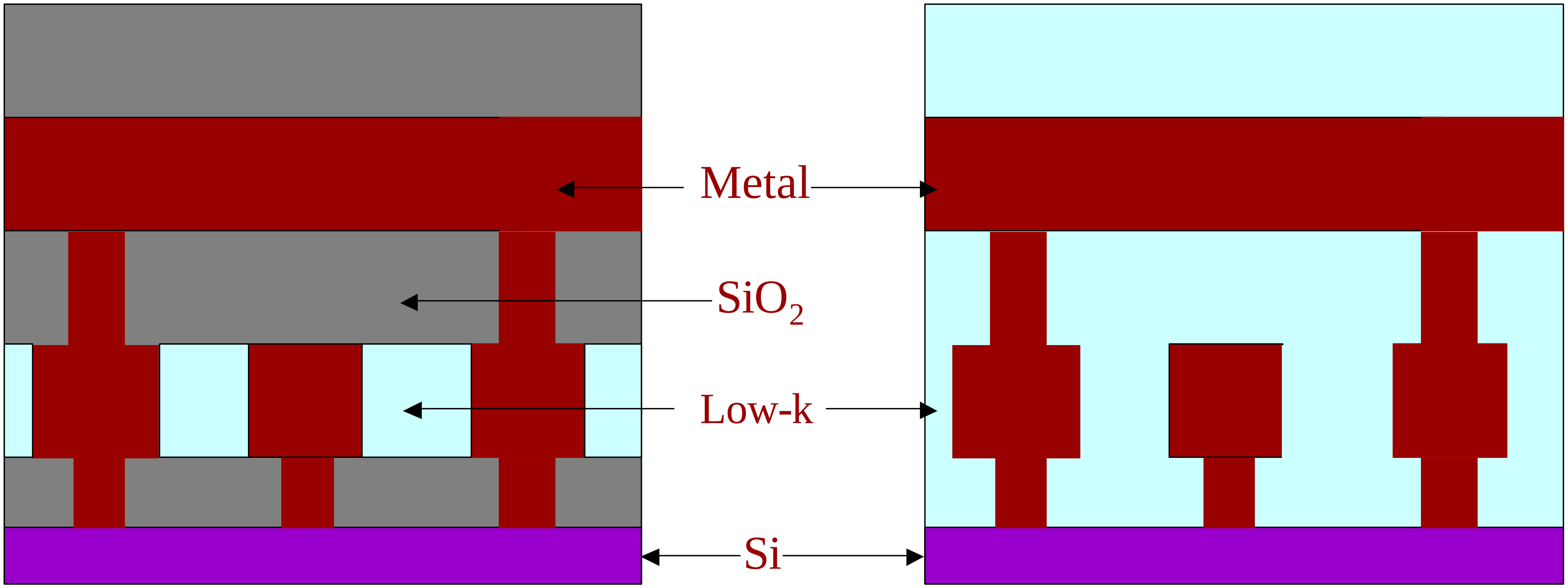
- **Metrics**
  - Delay
  - Power dissipation
  - Cross talk (data reliability)
  - Bandwidth
  - Area
  - Reliability



From ITRS

- **Mitigating Solutions (Technology)**
  - Al to Cu
  - lower k: Two Methods

Dielectric Technology



Non-homogeneous

Homogeneous

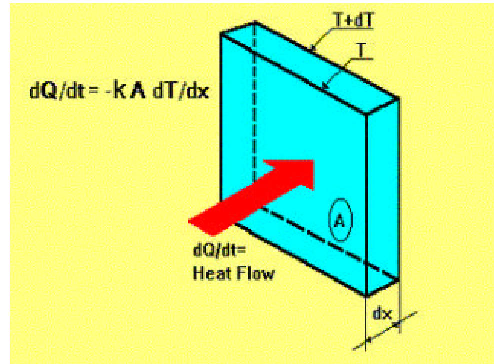
- Power: Homogeneous
- Cross talk: Non-homogeneous
- Delay:
  - local: C (homogeneous)
  - long distance: RC (Unclear?)

Self-Consistent Temperature Distribution

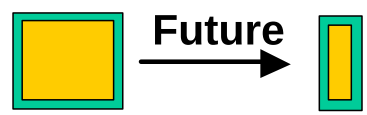
- Fourier's Law

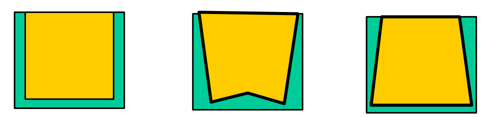
Ignored Before

$$J^2 r[T] \propto k_{eff}[T] \frac{dT}{dx}$$

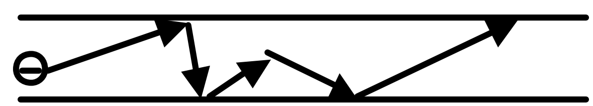


- Electrical Resistance ∝ r[T]
  - Thermal Coefficient of Resistance
  - Barrier, Surface Scattering
  - Number of metal levels



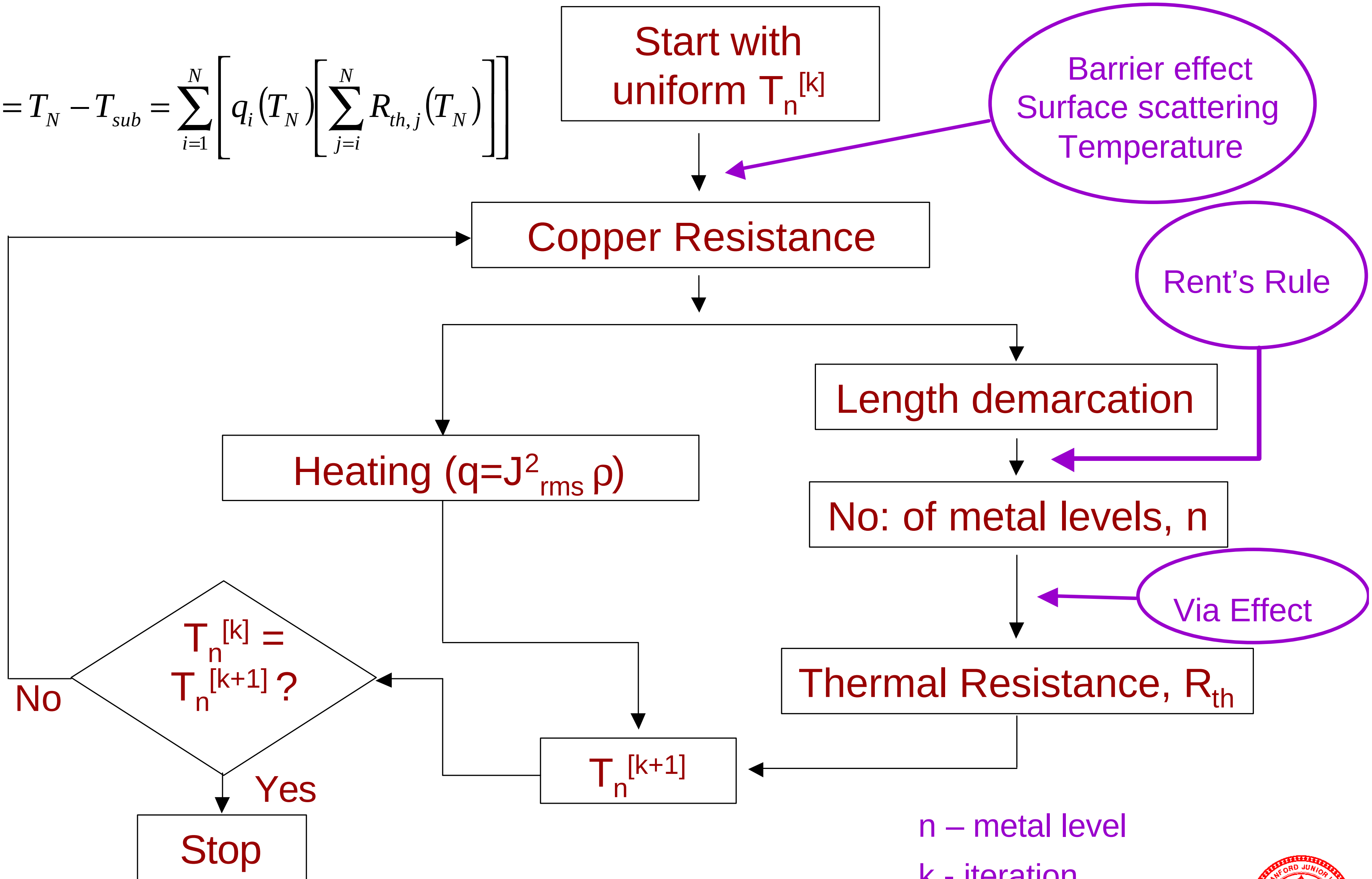


- Thermal Resistance ∝ $1/k_{eff}$[T]
  - Number of metal levels
  - Via Effect



Given Current Density, J. Find Temperature, T?

$$\Delta T_N = T_N - T_{sub} = \sum_{i=1}^{N}\left[q_i(T_N)\left[\sum_{j=i}^{N} R_{th,j}(T_N)\right]\right]$$

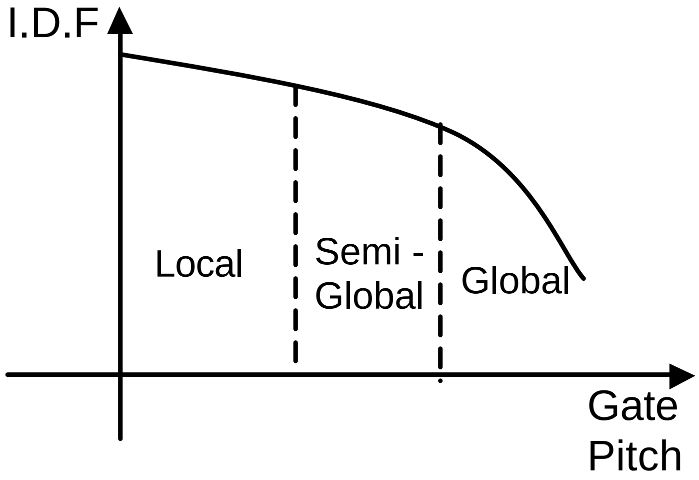


n – metal level

k - iteration

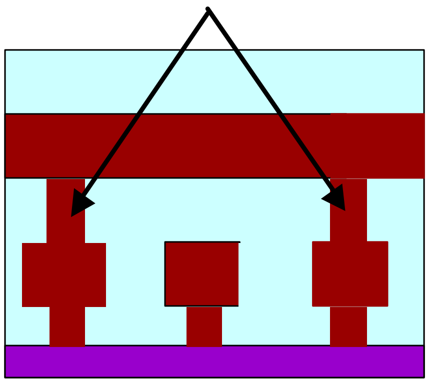
Electrical & Thermal Resistance

- Rent's Rule
  - Wire Length Distribution
- RC Wire Delay
  - Local, Semi-global, Global Demarcation
  - Number of metal levels
  - Stack Height

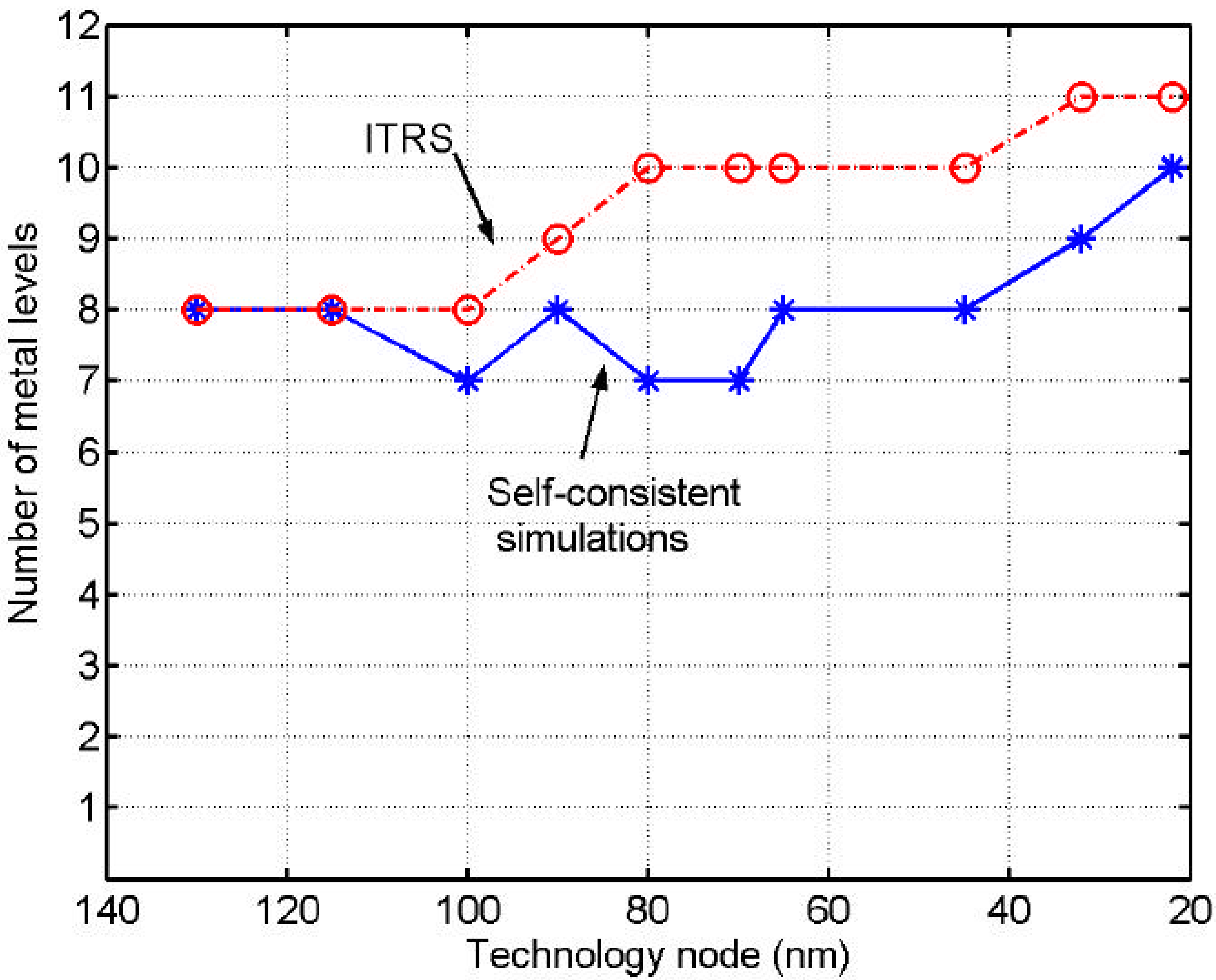


- Thermal Resistance
  - Stack Height
  - Via Effect

Efficient heat conductors
(reduce thermal resistance)



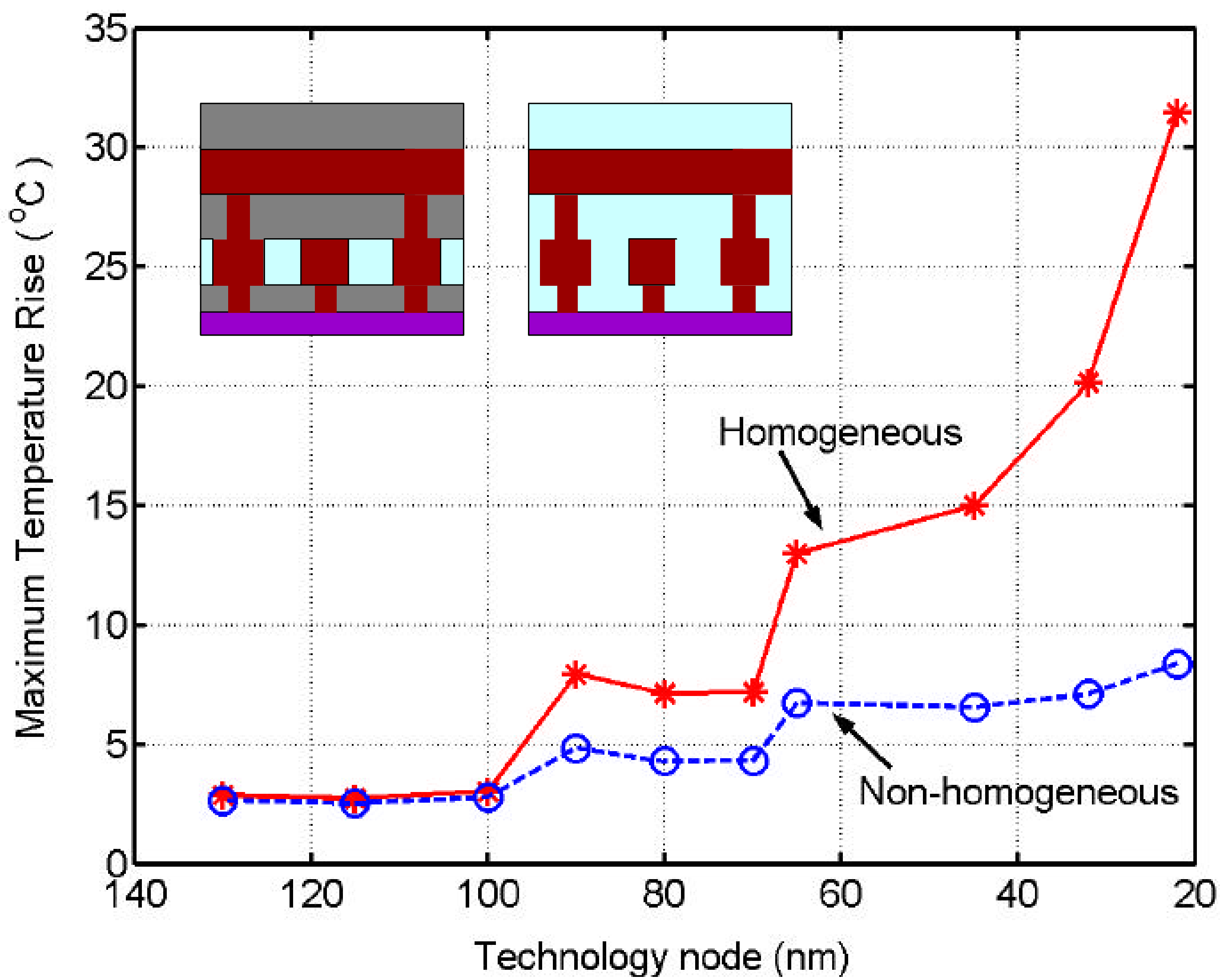
Number of Metal Levels



Fluctuations are artifacts of numerical calculations

Power, Ground & Clock lines not included

Maximum Temperature Rise $\Delta T \propto J^2 \rho \times R_{Th}$

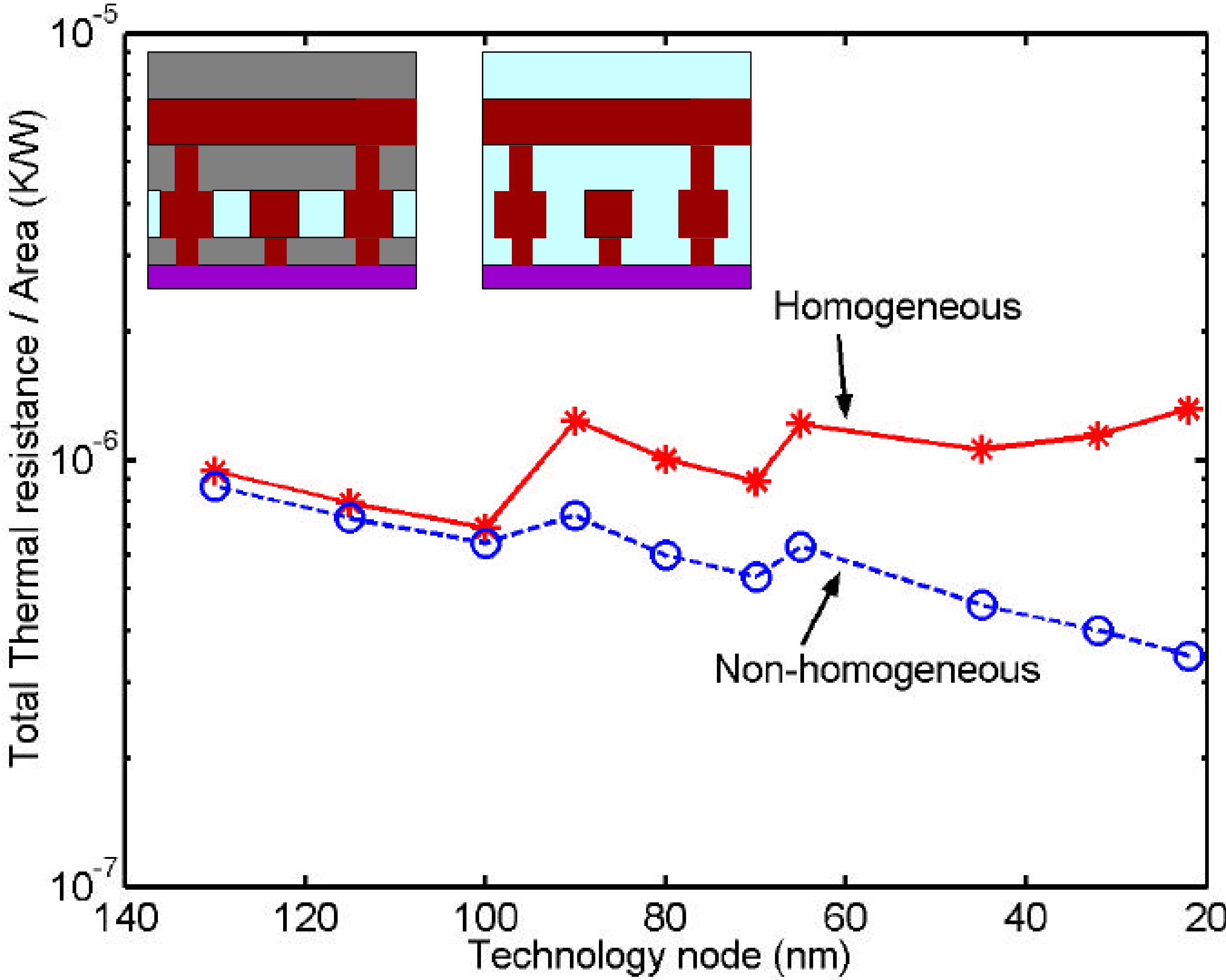


$\Delta T \sim 10\times \uparrow$

$\Delta T \sim 3\times \uparrow$

Effective Thermal Resistance

$R_{th,eff}=\Sigma H_i / K_{eff,\,i}$



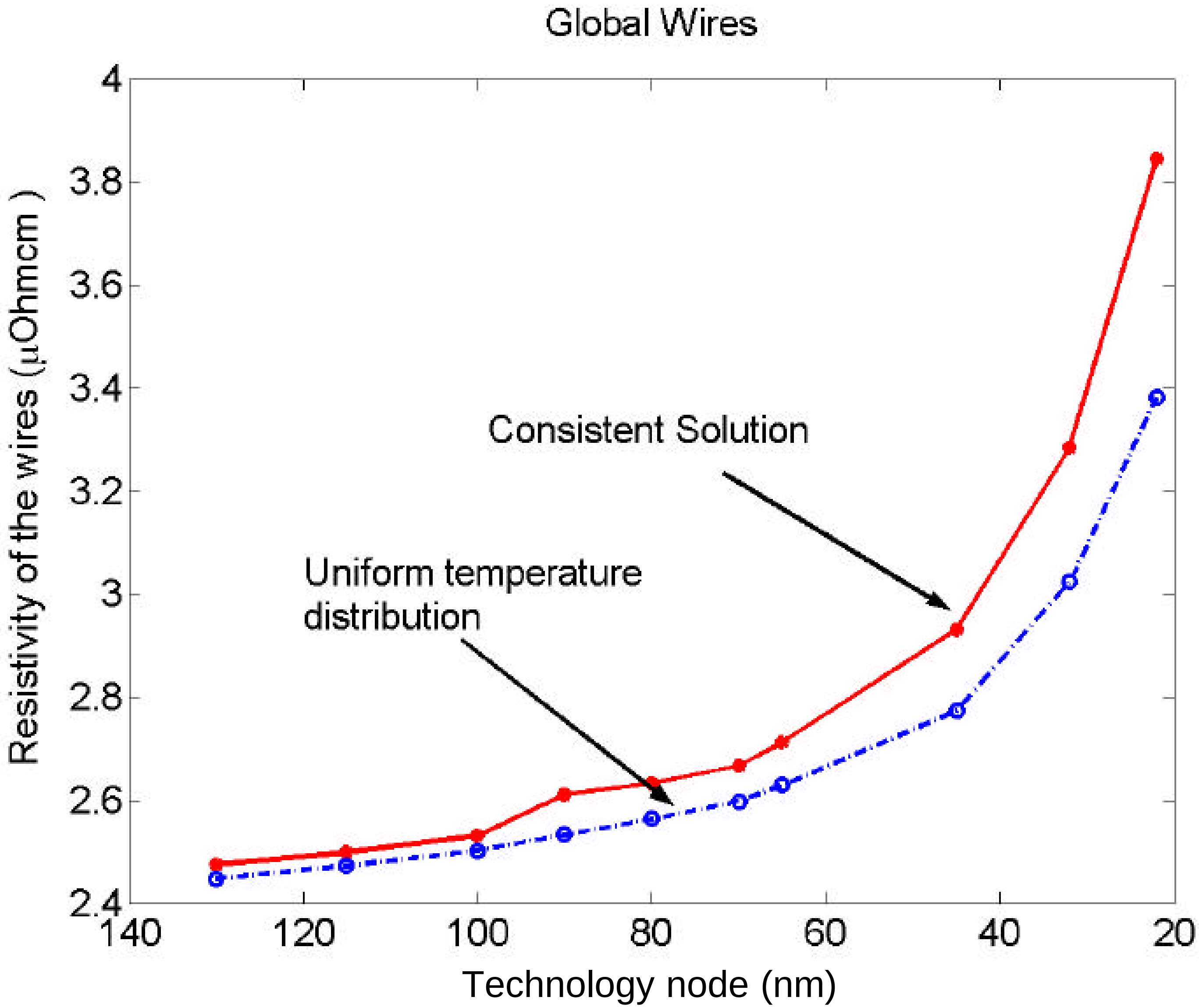
Surprising decrease!

Wire thickness
H ~ 4× ↓

$R_{th,eff}$ ~ 1.5× ↑
K_{eff} ~ 3.5× ↓
Poor Conductivity of Low-k

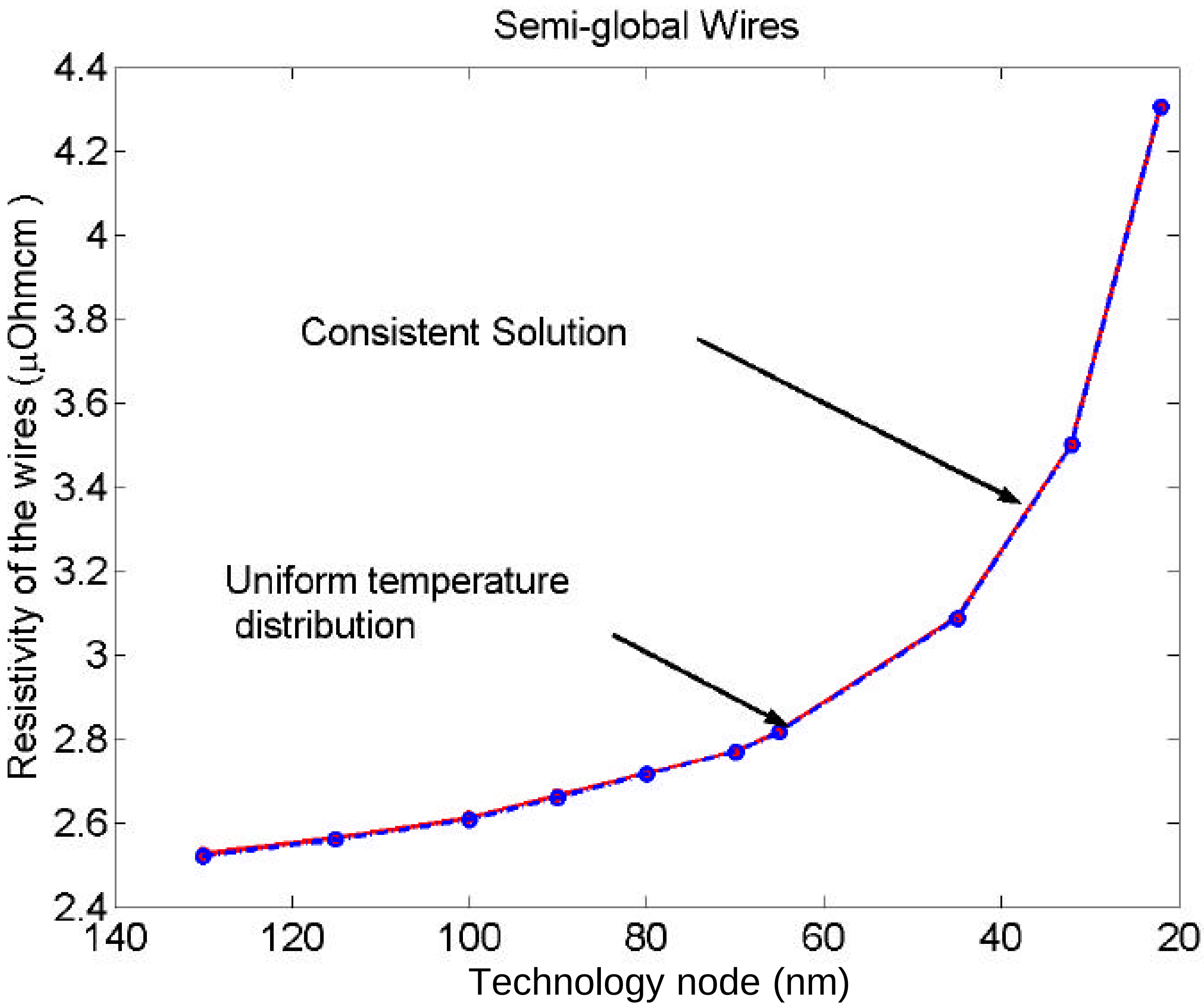
$R_{th,eff}$ ~ 3× ↓
K_{eff} ~constant
High Conductivity of SiO_2

Electrical Resistivity-Global Wires



Consistent Solution is larger by up to 15%

Electrical Resistivity-Semi-Global Wires

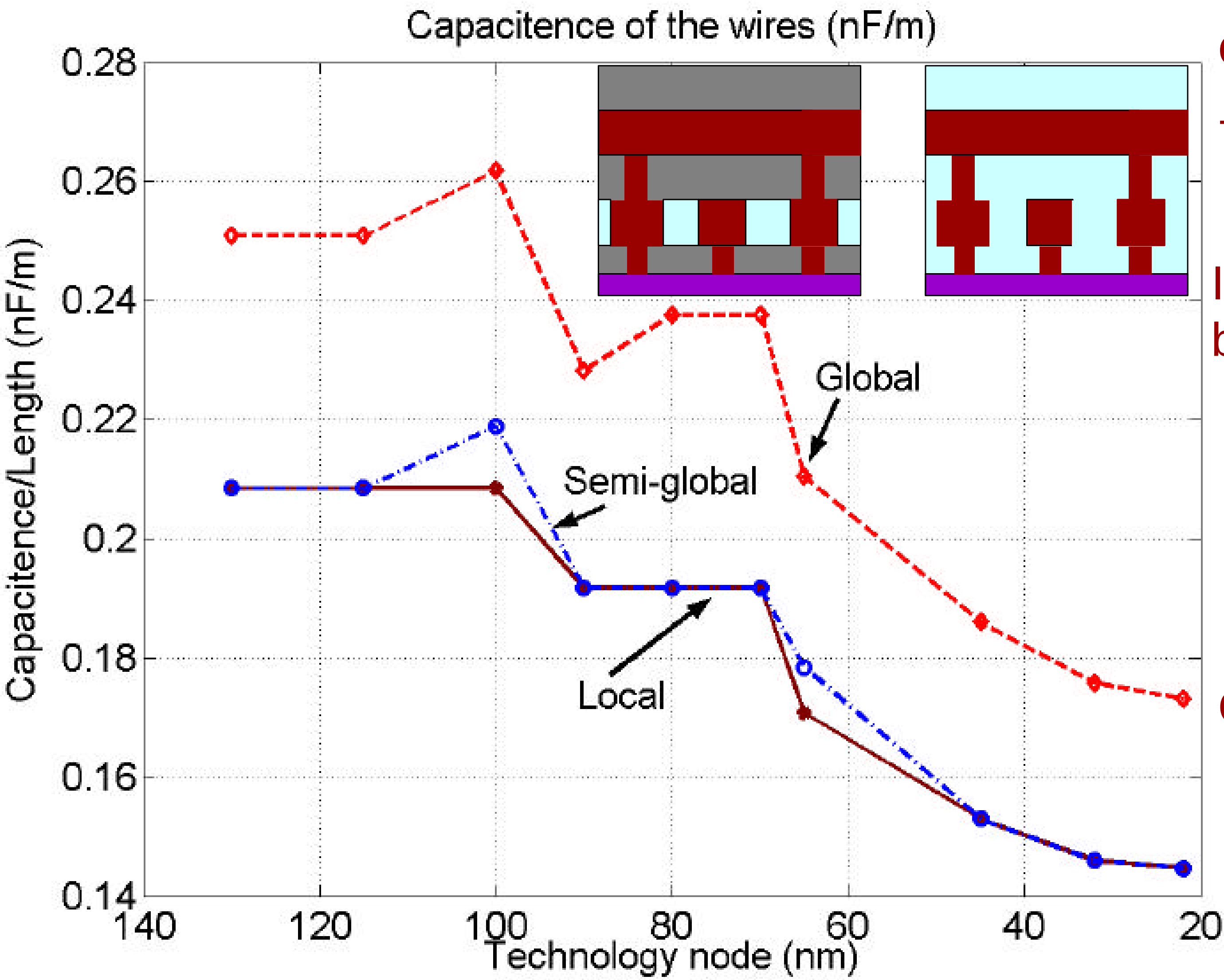


Negligible difference

Wire Temperature ~ Substrate T

Smaller wire pitch
⇒ Larger via density

Wire Capacitance



$C_{total} = C_{IMD} + C_{ILD}$

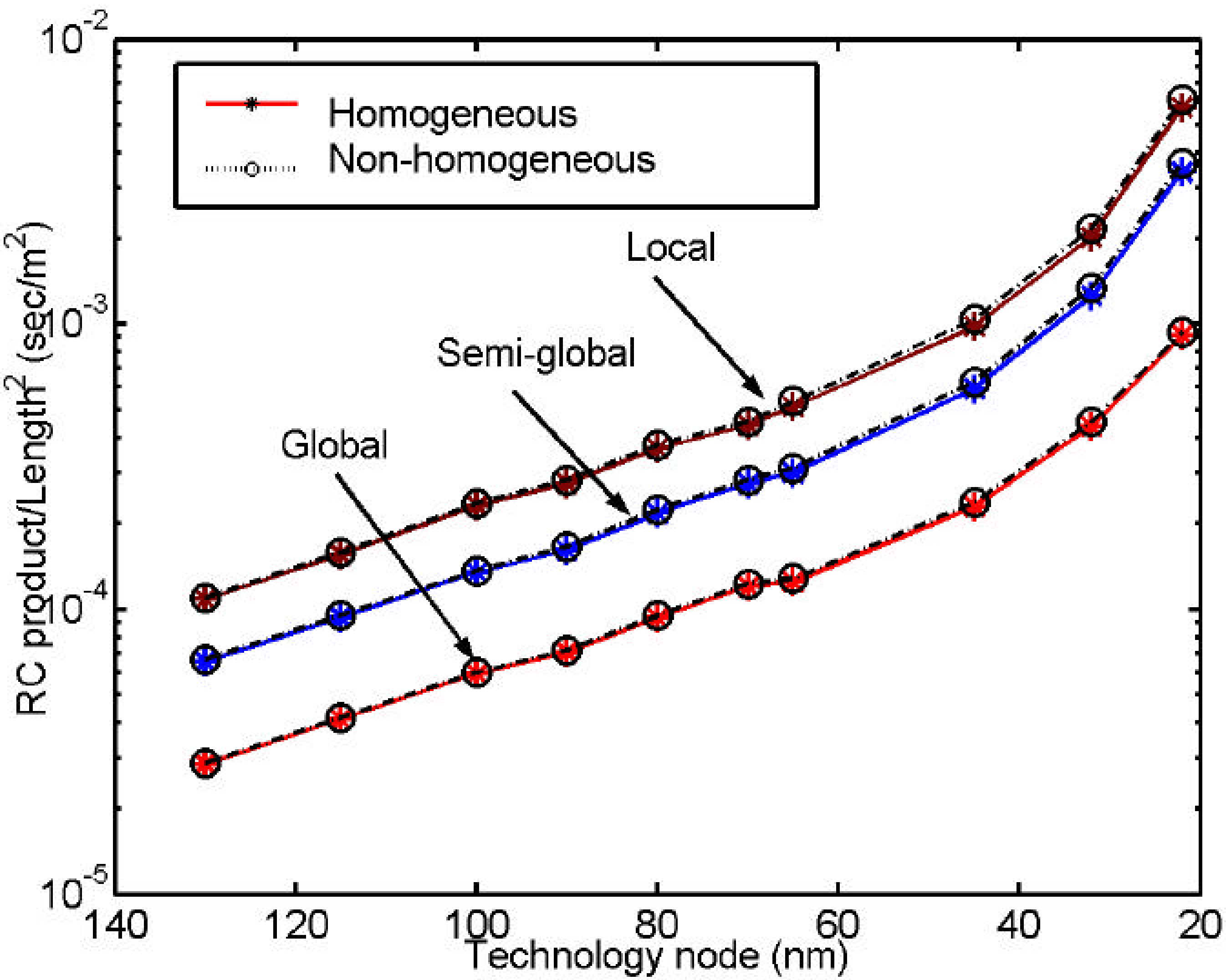
70% of $C_{total} = C_{IMD}$

IMD is Low-k for both cases

Capacitance 1.6× ↓

e_{IMD} ~ 2× ↓

Delay Metric - RC/L^2



R/Length ~ 50× ↑
C/Length ~1.6× ↓

Capacitance advantage of homogeneous is offset by the increased resistance

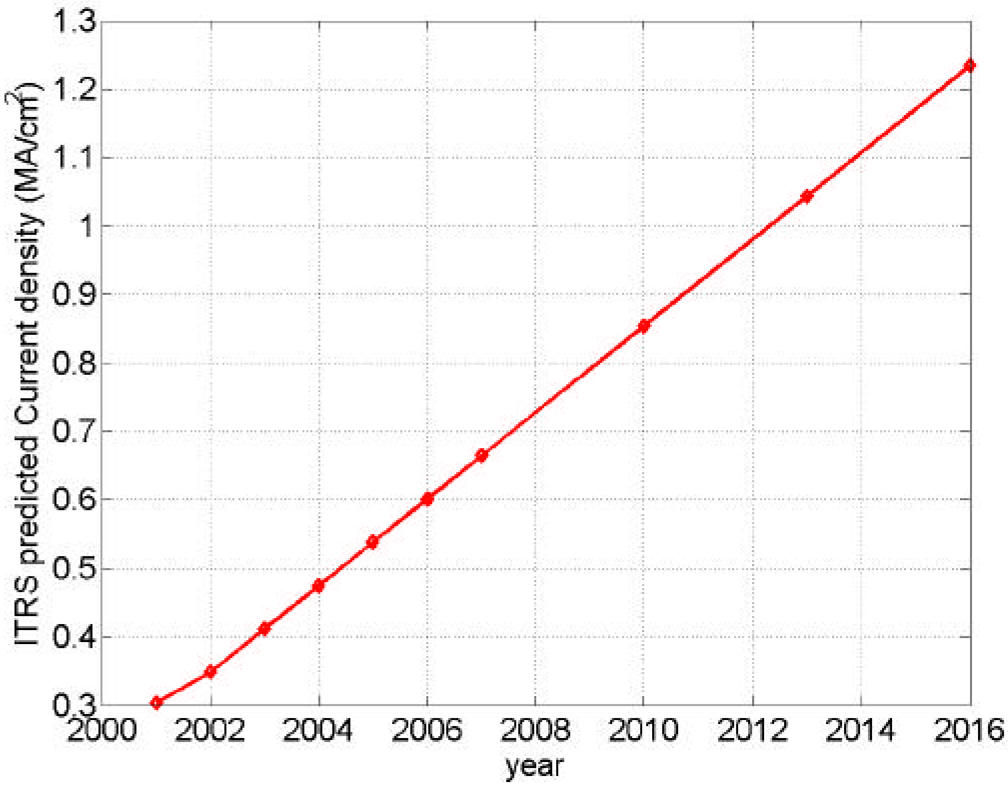
Is that all?
Reliability

Can Current Density go on Increasing?

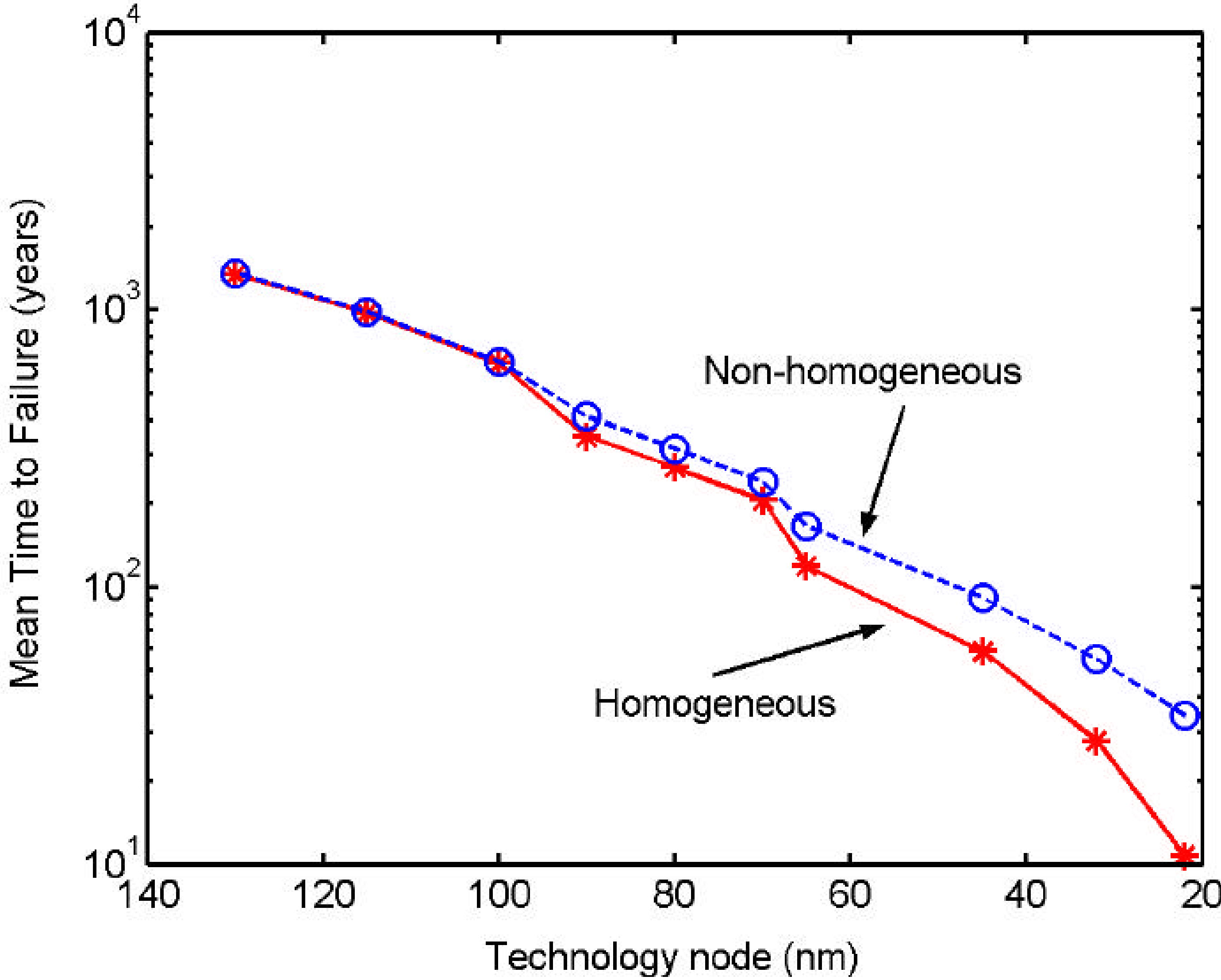
- Required Current
  - Integration density
- Allowed Current
  - Electromigration
  - IR drop in supply voltage
- Black's Law

$$MTF = AJ_{avg}^{-n} \exp\left(\frac{E_a}{kT}\right)$$

If J ↑⇒ T ↑ ⇒MTF↓



Mean Time to Failure



Larger Temperature
⇒ Lower MTF

Non-homogeneous is better.

- Reliability
- Cross-talk

$$X_{talk} \propto \frac{1}{1+\frac{e_{ILD}/e_{IMD}}{A.R^2}}$$

Is there a consistent solution?

- Black's Law

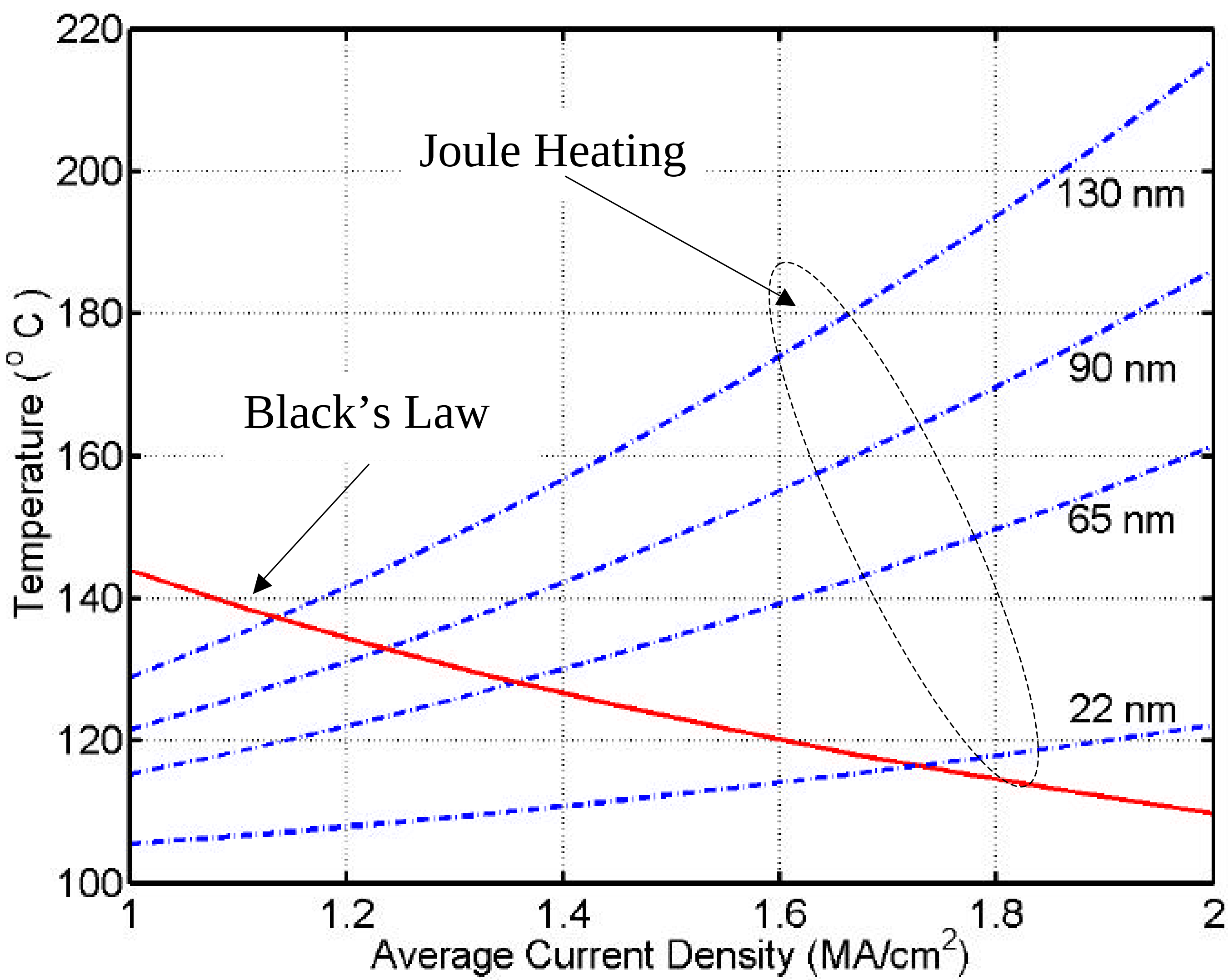
$$MTF = AJ_{avg}^{-n} \exp\left(\frac{E_a}{kT}\right)$$

- Joule Heating

$$J_{rms}^2 r[T] \propto k_{eff}[T]\frac{dT}{dx}$$

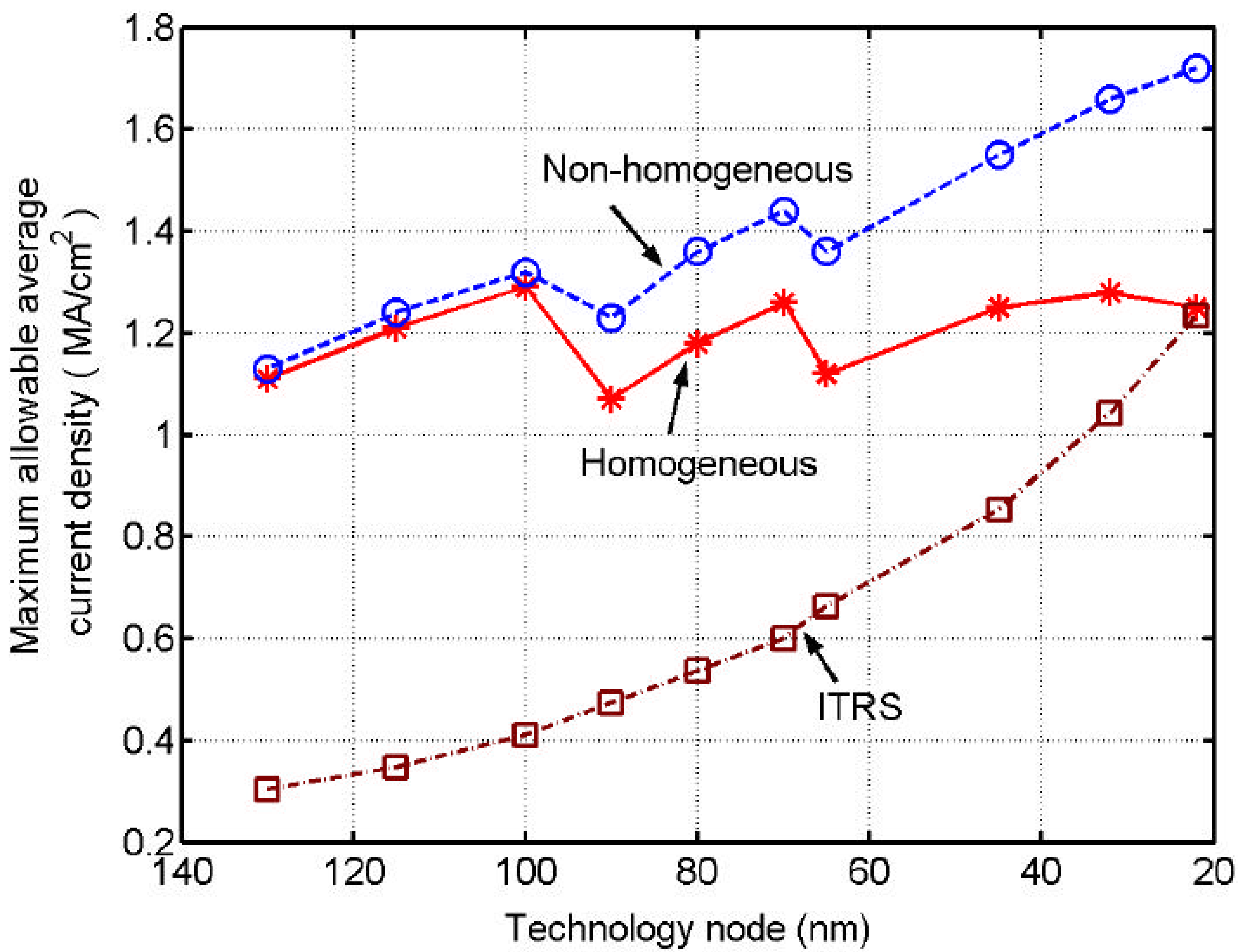
$$J_{avg}^2 = rJ_{rms}^2$$ r - Duty Cycle

Consistent Solution



Point of intersection
is the consistent solution

Consistent Solution



Conclusion

- Consistent Algorithm to estimate
  - Thermal Profiles
  - Electromigration constraints
- Comparison of Dielectric Technologies
  - Power, Delay - Homogeneous
  - Cross-talk, Reliability – Non-homogeneous

Thank You