Placement Rent Exponent Calculation Methods, Temporal Behaviour, and FPGA Architecture Evaluation

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Some Questions

- How best to calculate placement Rent?
- Are there biases in calculation methods?
- How does Rent exponent change with timing-driven placement?
- Do circuit “types” have a common Rent characteristic?
- How does Rent exponent change with placement quality?
Goals of this paper

- Purely empirical study.
  - Many benchmarks, different sizes.
  - Commercial FPGA architecture.
  - Looking for interesting trends in the data.
- Try to address the preceding questions.
- Look at FPGA architecture wiring requirements and Rent’s Rule.
Applying Rent’s Rule: \( P = kB^r \)

- One circuit:
  - Estimate wirelength, pre-placement.
  - Extract \( r \), follow models for wirelength.

- Many circuits:
  - Estimate wirelength required for an FPGA architecture.
  - Extract a “typical \( r \)”.
  - Did we provide enough interconnect at each level of “hierarchy”? 
FPGA Architecture

Cyclone C6

How many?

How many?

How many?
Motivation: Apex Rent Exponents

APEX 20K400

\[ P = 0.5854B + 1.694 \]

\[ R^2 = 0.6215 \]

\[ P = 0.6522B + 1.8435 \]

\[ R^2 = 0.6215 \]
Questioning the methodology:

Contribution to Rent exponent

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Calculating Rent Parameters

- **Partitioning Rent:**
  - Matches the APEX CAD flow and architecture

- **Placement Rent**
  - More relevant to a placed circuit.
  - Feuer: for a good placement, a “sample” of the placement should behave as Rent.

- **But what is a “sample”?**
  - Hypothesize that the definition of the sample will affect both the results and spirit of the analysis.
I. Partition-based
II. Random x-y region
III. Random $x$-$y$ + lengths
IV. Random x-y + radius
“Region” Size

Is it “fair” that smaller samples contribute much more heavily to the Rent parameter?
Is it “fair” that some cells of the placement contribute much more heavily to the Rent parameter?
Rent exponents differ with method
Significantly…

Comparison of final Rent exponent

Design
Preconceived biases

- Placement cost function is:
  - Minimum wire usage
  - Best worst-case path delay
- Placer is simulated annealing based

A priori belief that RND\_xy\_rad should be a more accurate reflection of the placement quality / architecture stress.
Conclusions on sampling methods

- The straightforward way of measuring does not “seem” fair.
- Other methods seem more natural.
  - If you believe in applying Rent to a non-partitioning situation.
- Significant variation in measured r based on the method used.
- Question: what does this mean?
  - Unfortunately, no answer for this.
Design Characterization.

Parameter \( r \) varies with the “structure and type of circuit”? 

![Graph showing Rent Parameter by Design Type with categories: control logic, dsp, image, networking. The bars represent the variation of the parameter across different design types, with a red line indicating a threshold or average value.]
Timing-driven placement

- Pushes out both Rent ($r$), wirelength ($w$).

If you measure $r, w$ with a partitioner, but apply it to a timing-driven placer, results will differ.
Complicating observation.

- Both $r$ and $w$ move, but not necessarily together.
Temporal correlation

For a given circuit, decrease in $r$ over the course of placement correlates strongly with placement quality / wirelength!
Conclusions on time and wirelength.

- I don’t see a correlation between circuit type and r. It looks to be more complicated.
- TDC affects both r and w.
  - But not in lock-step.
- *If* you start with normalized r and w, the two are surprisingly correlated as the placement quality improves.
  - Does this apply outside of the simulated annealing world?
Predicting wirelength

Simple goal: how well does a naïve model work for FPGAs?

Answer: random scatter, until we adjust the model for the architecture, then “reasonable”
Rent and Cyclone

- Rent used only as a guiding principle in designing Cyclone – almost entirely empirical.
- Rent exponent of the device is .72, while the average in the design set is .55.
Easy and hard designs

- The Rent exponent of the architecture is safely above the most stressed design.
  - Almost exactly $\bar{r} + 2\sigma$

- Note worst-case vs. average case. We do not consider Cyclone to be over-routed.
Segmented Rent Plot

- Rent parameter of cyclone is NOT 0.72.
- LABs have input 26, output 10, size 10.
- 80 global tracks in H and V direction.

Wires increase with perimeter
Conclusions

- Empirical study.
- Importance of Rent methodology
  - Biases and effect on r,w.
- Measurement and correlation to FPGA architectures.
  - Naïve adjustment of Feuer works “OK”
  - Interesting Rent properties on Cyclone.
- Rent exponent and placement quality/time.
  - Stronger than expected correlation.