# Understanding Metrics in Logic Synthesis for Routability Enhancement

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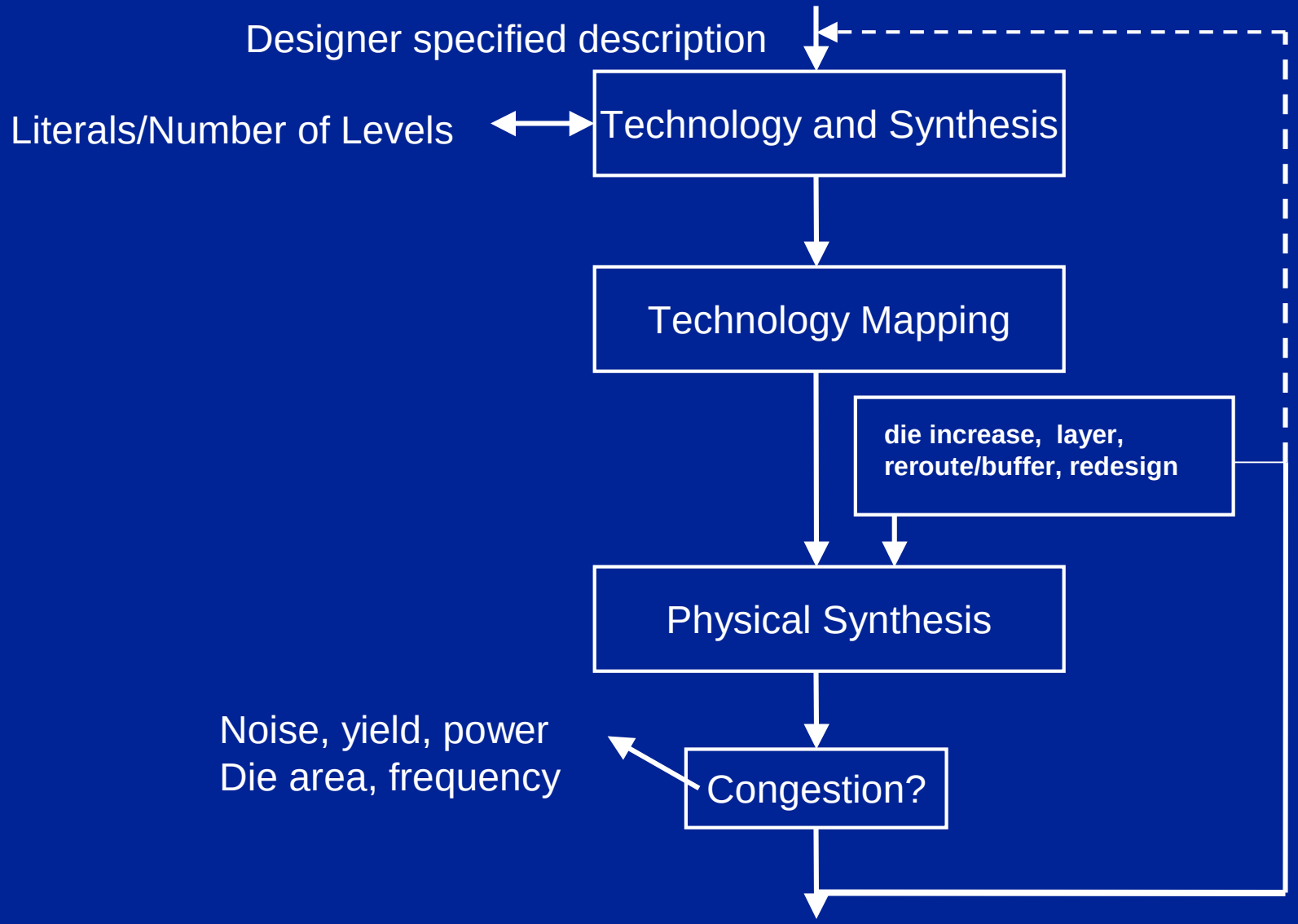
# Outline

- Motivation and approach
- Structural metrics
- Logic transformations
- Conclusions and future work

# The Route To Congestion



# Motivation

- Efficient use of design resources
- Improved routability
- Reduced turnaround time

# Metrics for Early Synthesis

- Much of the structure is determined during technology independent synthesis
- Literal count and number of levels are only metrics used
- None of these capture structure

# Approach

- Do “place-and-route” *predictions* early in the design flow
  - prediction on routability
  - predictions on congestion
- Make predictions at the *logic restructuring* level
  - use topological properties of a circuit
  - rely on accurate metrics
- Classify *logic transformations* in terms of their impact on circuit structure
  - transformations have “re-wiring” patterns
  - should be driven with structural metrics

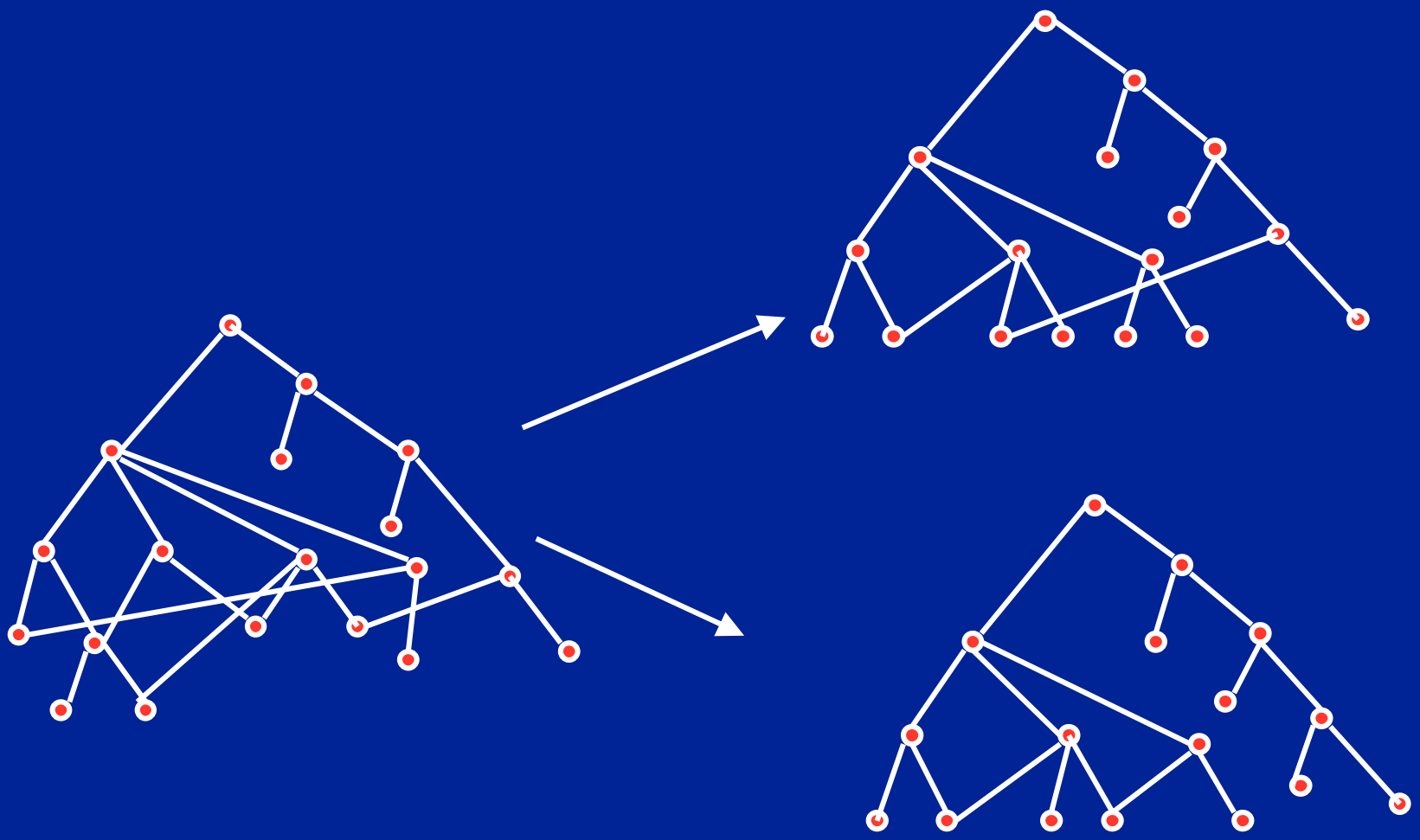
# Outline

- Motivation and approach
- **Structural metrics**
- Logic transformations
- Conclusions and future work

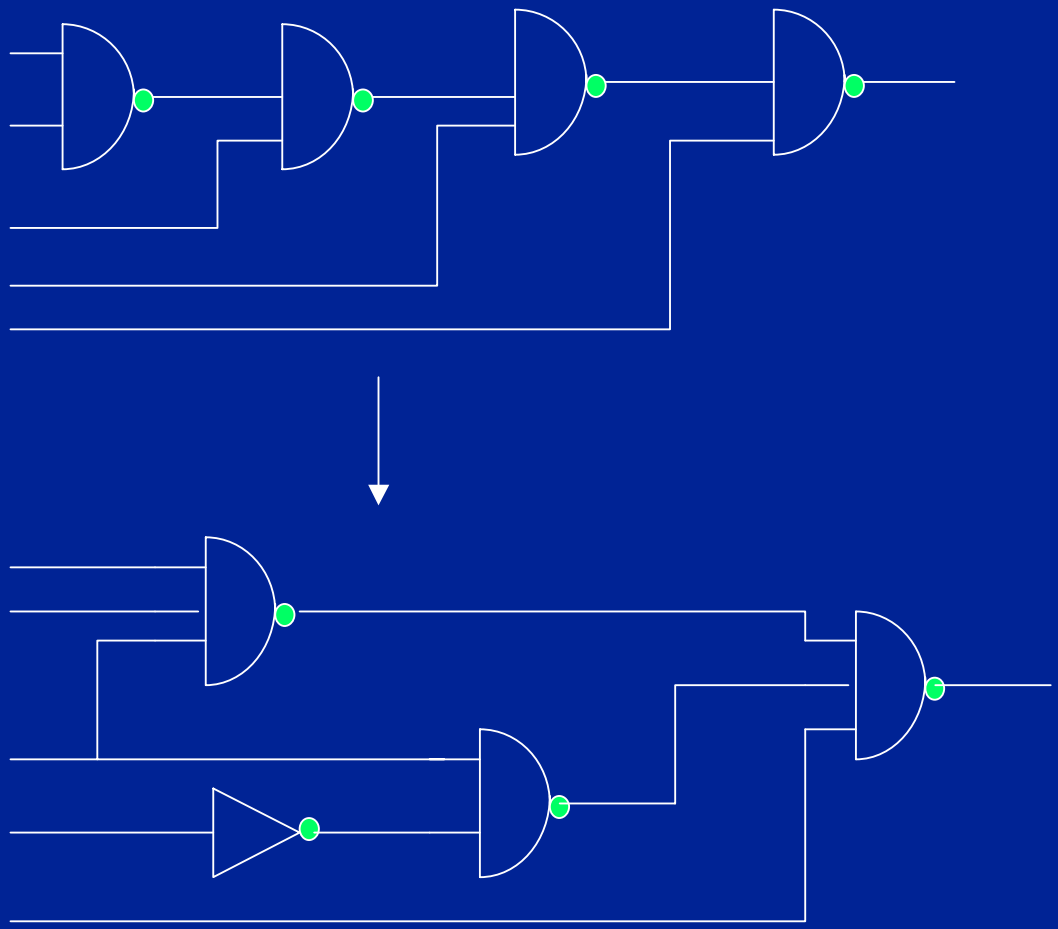
# Structure as Prediction

- Technology scaling and interconnect effects:
  - Regular Fabrics  eg: Pileggi et. al and Mo et. al.
  - Regularity and random logic eg: Stok et. al.
  - Wire Planning, eg: Gosti et al.
- Common idea with all approaches is that “structure” is important to quality of results
- But how is structure measured? Structure -> QOR correlation

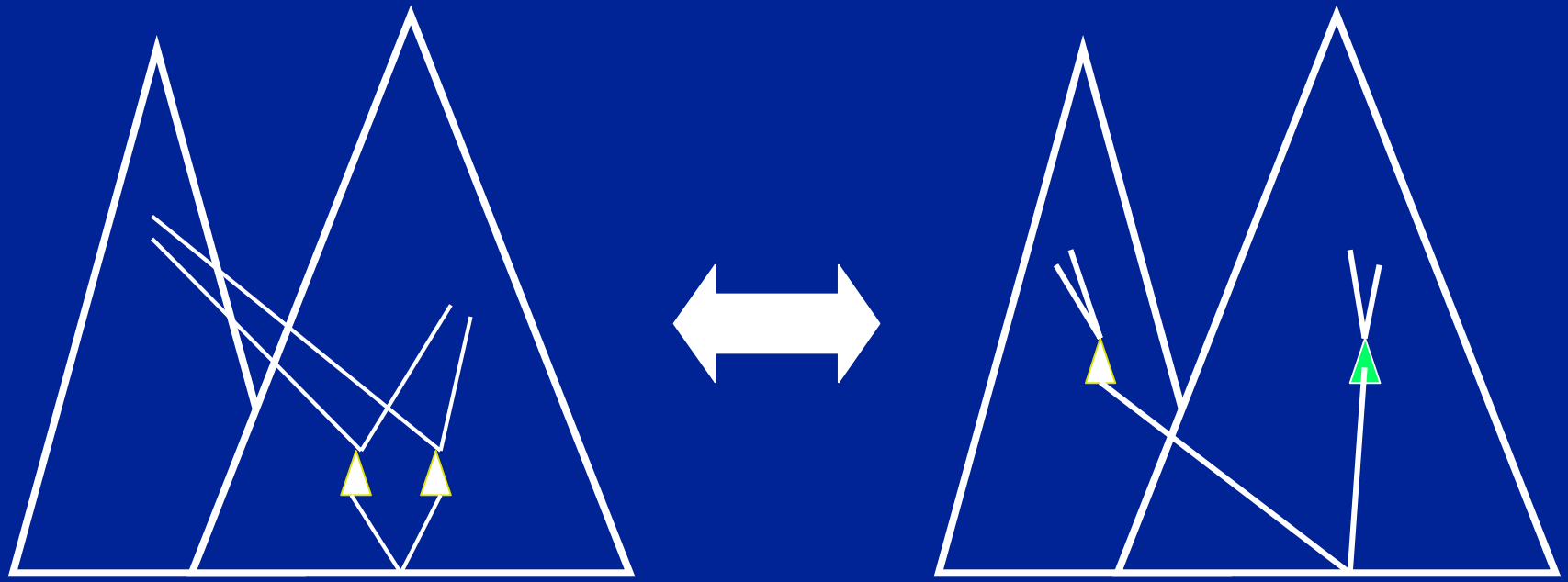
# Factorization



# Rewiring



# Fanout



# Problem Exploration

- Is there a property of network graph structure that contributes to routability?
- Can it be measured?
- Can such a measurement be used in optimization of logic networks?
- Can the metric be computed fast and incrementally?

# Graph Structure and Partitioning

- Relationship between graph structure and congestion: known work is that of Donath and Hoffman
  - Relates Eigen Vector to a crude lower bound on min-cut partitions
  - Lower and upper bounds interesting, but need real-time metrics
- “We need a set of properties, there may not be one single magic metric” Donath

# Requirements of a Metric

- Primary function
  - measures transformational changes to netlist
- Wish list
  - computation cost
  - Incremental

# Conjecture

- Is there a property of network graph structure that contributes to routability?
  - Yes

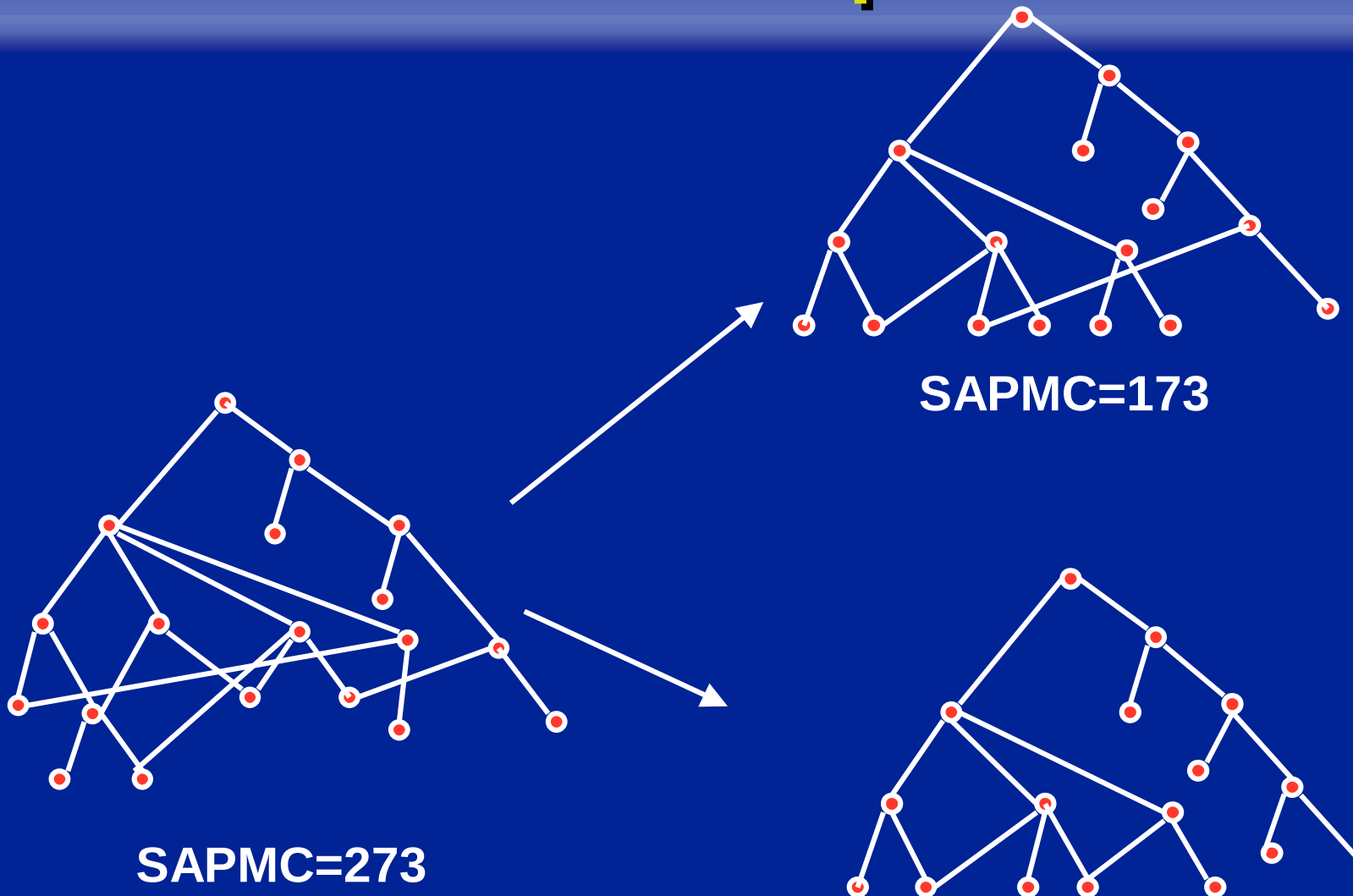
# Adhesion

- Significant research in areas like: communication, social theory,  internet, etc.
- Used to study issues : reliability, group dynamics, network structures, rates of growth etc.
- Adhesion in social theory
  - A group consists of members (vertices) and relations (edges)
  - A group is adhesive to the extent that multiple independent relations of its members are pairwise resistant to being pulled apart. (White & Harary)

# Adhesion in Logic Networks

- Adhesion of a logic network is the sum of the minimum number of edges between “all pairs” that if removed would disconnect the group
- Maps to a problem in graph theory with ongoing research for network reliability: SAPMC
- Adhesion = property, SAPMC = metric

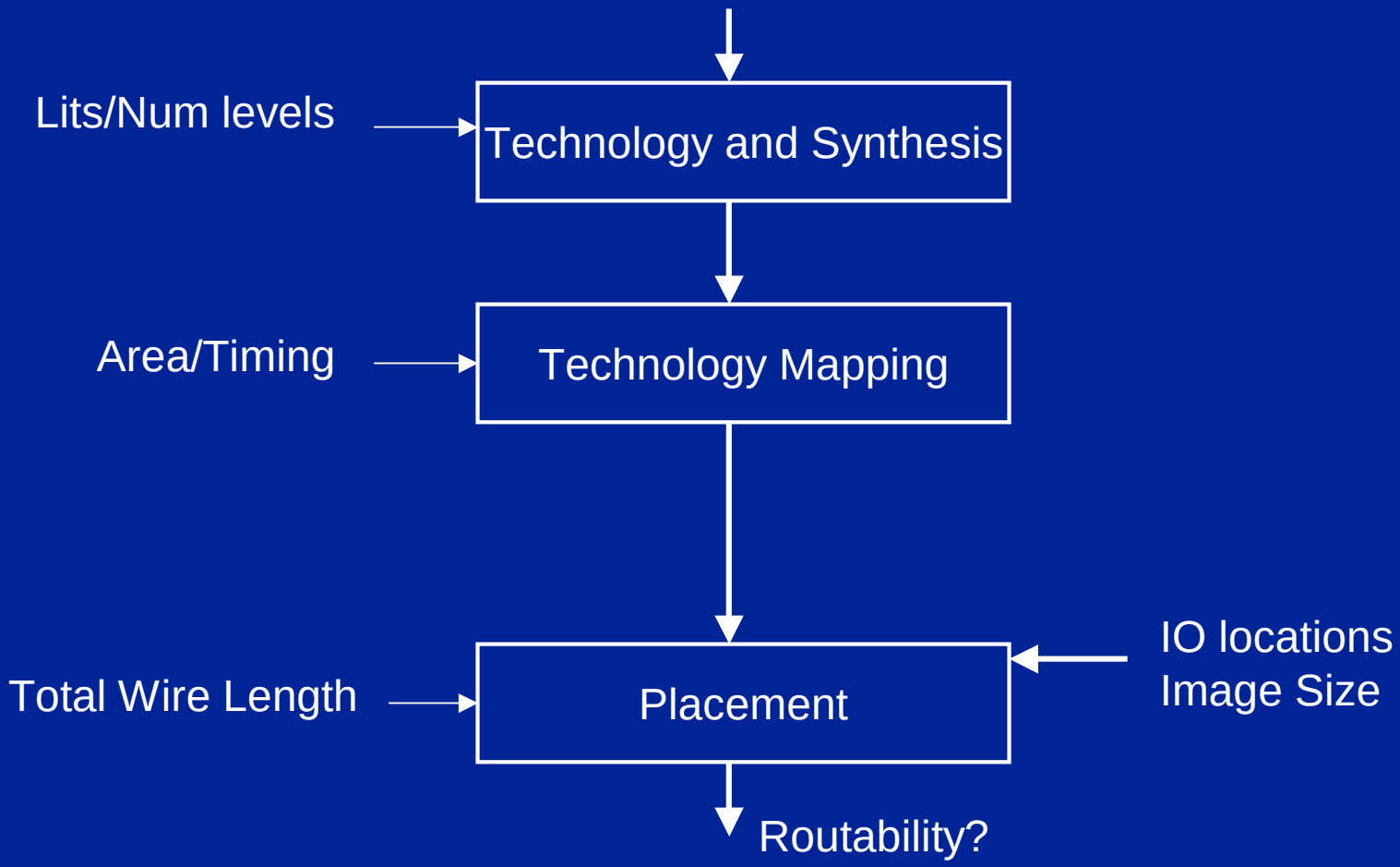
# Adhesion Metric Example



# Metric Goodness

- Can adhesion property be measured for logic networks?
  - How good is it as a predictor for congestion?

# Timing Closure Flow



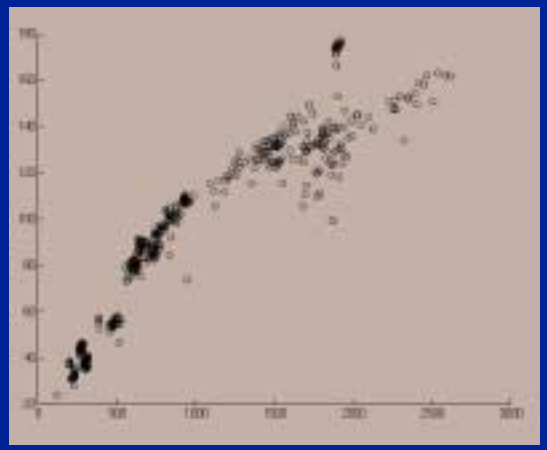
# Nature of Technology Independent Metrics

- Lower literal count metric *typically* correlates with improvement in post placement routability
- We expect:
  - Use of adhesion to improve the correlation with post placement routability

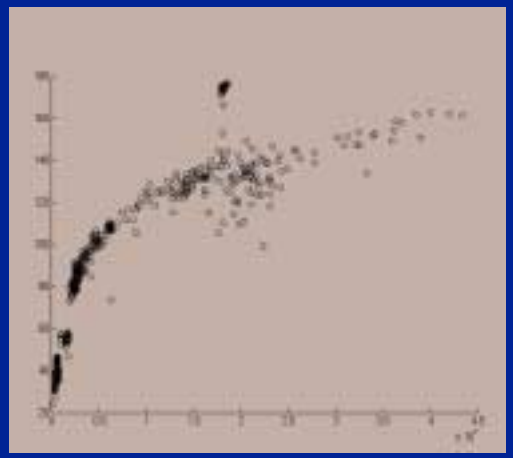
# Experiment

- To measure improvement in correlation with adhesion
- 27 benchmark circuits were considered
- Each example had 25 different technology independent implementations with *only one* optimization step modified
- Direct mapping to NAND2s
- Each of the designs points were placed 25 times with random IOs to account for their contribution
- 27x25x25=16875 data points were considered

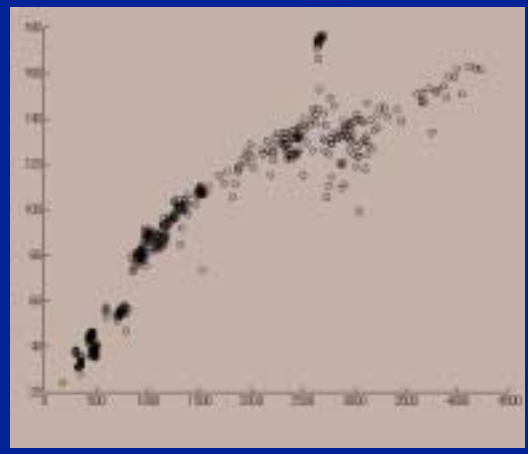
# Correlation of Potential Metrics



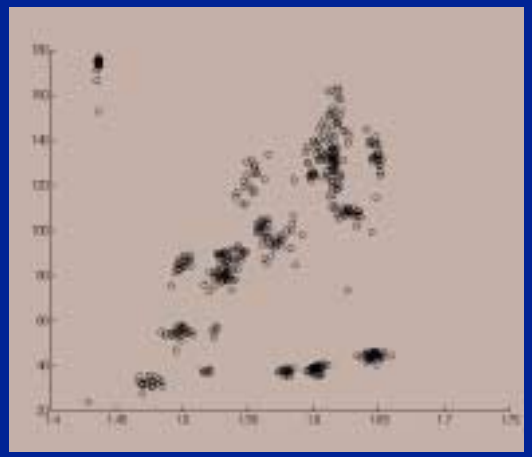
Literal Count



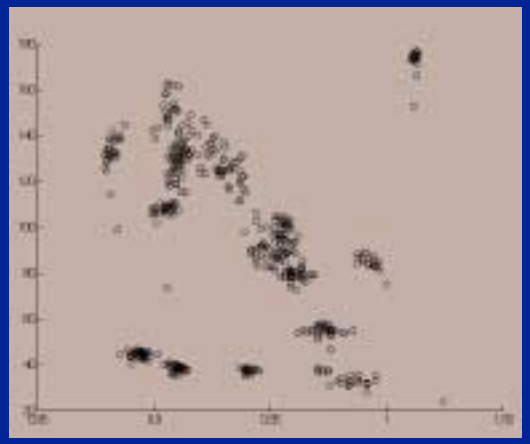
Adhesion



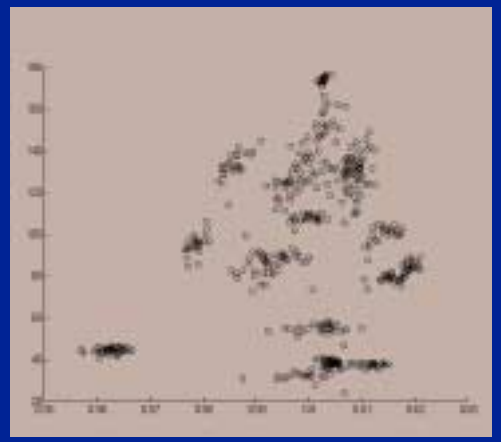
Area



Average Fanout



Level Metric



Literal Density

# Individual Variable Correlation

Table 1: Max Congestion Fit

| Variables | R. square | Residual Std. Error |
|---|---|---|
| Literals | 0.844 | 23.46 |
| Num of Cells | 0.866 | 21.70 |
| Adhesion | 0.643 | 35.46 |
| Levelization Metric | 0.404 | 45.86 |
| Normalized APMC | 0.086 | 56.79 |
| Average Fanout | 0.077 | 57.05 |
| Literal Density | 0.007 | 59.18 |

# Stepwise Correlation

**Table 4: Stepwise Regression**

| Model | Max Con | Avg Cong | TWL |
|---|---|---|---|
| $f(L)$ | 0.841 | 0.825 | 0.942 |
| $f(L, C)$ | 0.932 | 0.922 | 0.961 |
| $f(L, C, A)$ | 0.984 | 0.983 | 0.998 |
| $f(L, C, A, B)$ | 0.988 | 0.987 | 0.999 |
| $f(L, C, A, B, L_d)$ | 0.989 | 0.988 | 0.999 |
| $f(L, C, A, B, L_d, F)$ | 0.990 | 0.989 | 0.999 |
| $f(L, C, A, B, L_d, F, 0)$ | 0.993 | 0.991 | 0.999 |

# Optimization Using Adhesion

- Can such a measurement be used in optimization of logic networks?
  - Yes, SAPMC can be used in optimization of logic networks as secondary metric

# Experimental Setup

- 20 examples considered
- Only one optimization was changed, i.e, factorization
- Two implementations one which includes adhesion cost, one without.
- Adhesion used a tie breaker
- Placed 25 times, with random IO locations

# Optimization Results

Table 5: Modified $f_x$ Optimization Results

| Circuit | $MC_{nor}$ | $MC_{mod}$ | $APMC_{nor}$ | $APMC_{mod}$ |
|---|---|---|---|---|
| C880 | 63 | 61 | 681128 | 643362 |
| S420 | 25 | 25 | 40375 | 40375 |
| C17 | 8 | 8 | 205 | 205 |
| S820 | 66 | 63 | 328125 | 321772 |
| S641 | 44 | 42 | 160944 | 158527 |
| S382 | 32 | 28 | 95789 | 76108 |
| S349 | 36 | 35 | 81619 | 79222 |
| C1908 | 79 | 67 | 781140 | 763519 |
| S838 | 30 | 30 | 154769 | 154769 |
| C432 | 75 | 72 | 629335 | 621463 |
| S1423 | 107 | 83 | 2458040 | 2202390 |

# Experimental Observations

- The contribution of circuit structure to congestion can be measured
- Circuit structure can be improved for routability
- Literal count and number of levels not sufficient anymore, need an additional metric for structure

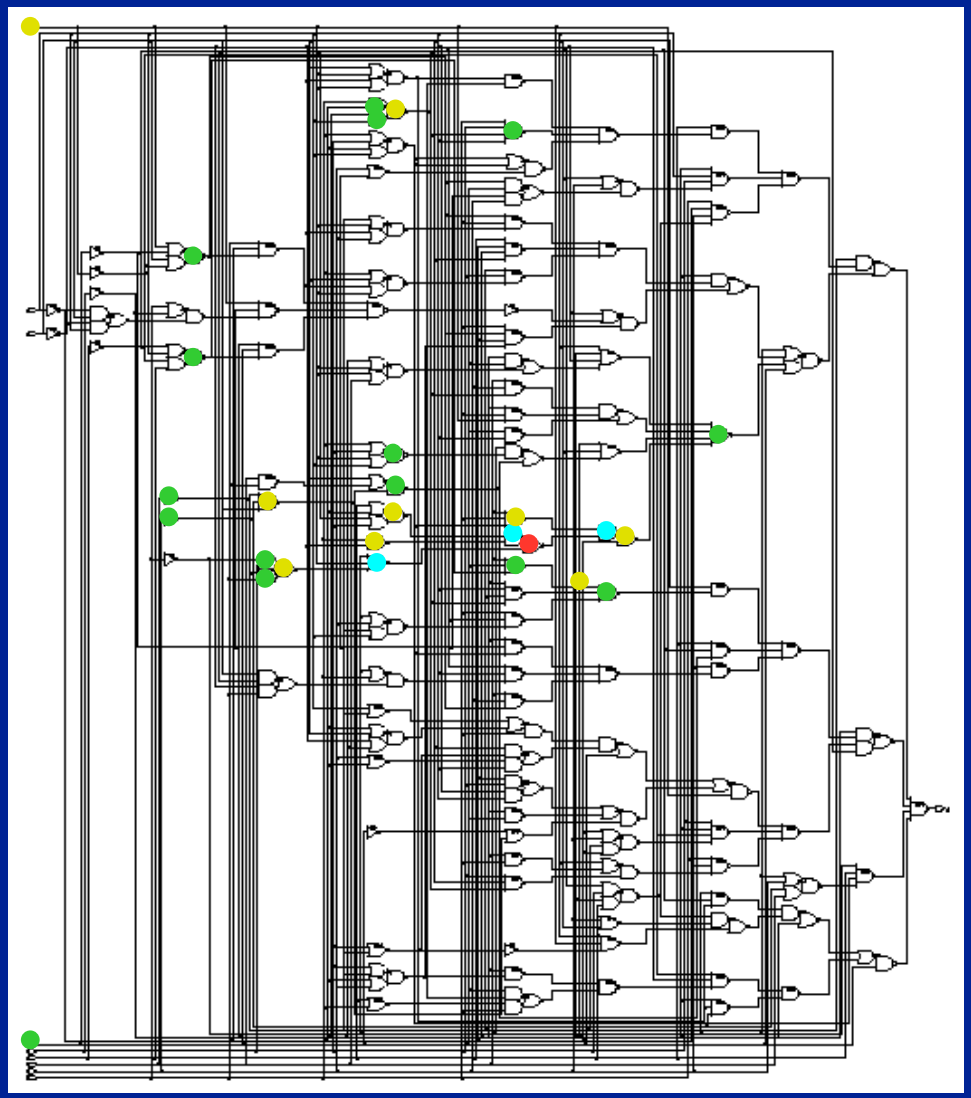
# Incrementality of Metric Computation

- Can SAPMC be computed fast and incrementally?
  - Not without approximations. However there are heuristic metrics for adhesion.
- Other metrics?

# Distance Metric [Heineken95]

- Uses notion of *neighborhood population* that is computed relative to a given cell and distance *k*
- For each *k* computes neighborhood population across all circuit cells and then averages them
- In the past was used for yield estimation

# Distance Metric Example



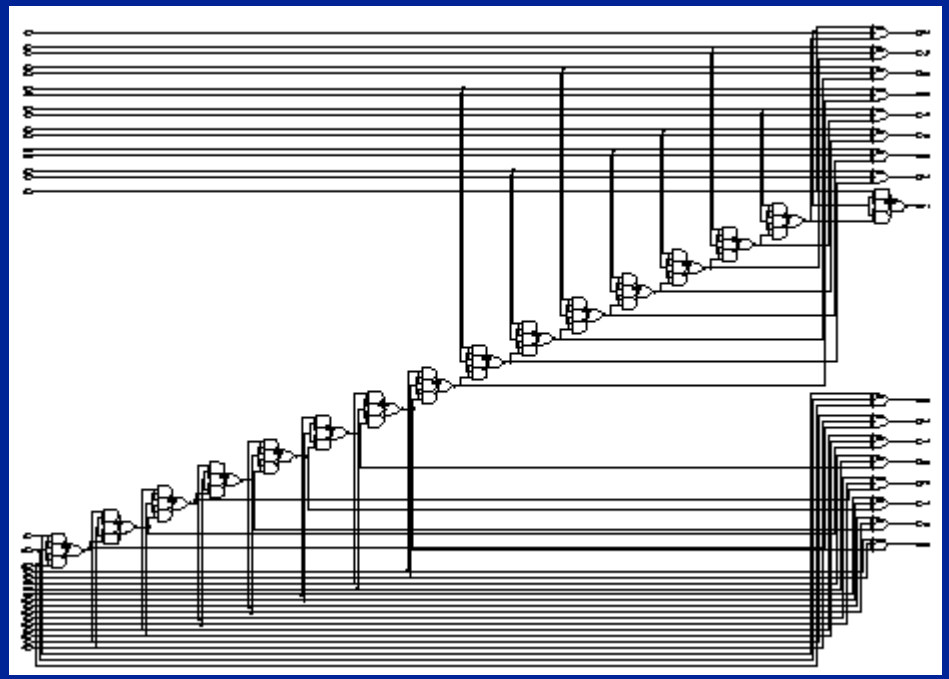
- given cell
- distance 1 (3 cells)
- distance 2 (9 cells)
- distance 3 (15 cells)

**Avg. across all cells:**

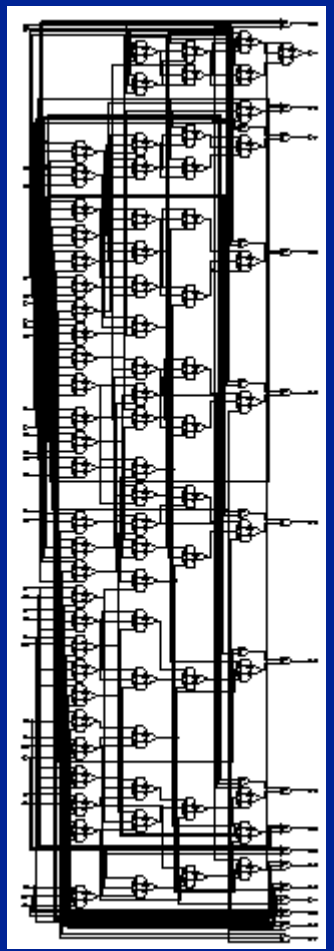
`1:2.8  2:6.9  3:7.5  4:7.8  … 10:4.3  11:0.0`

# Two Structural Variants of Adder

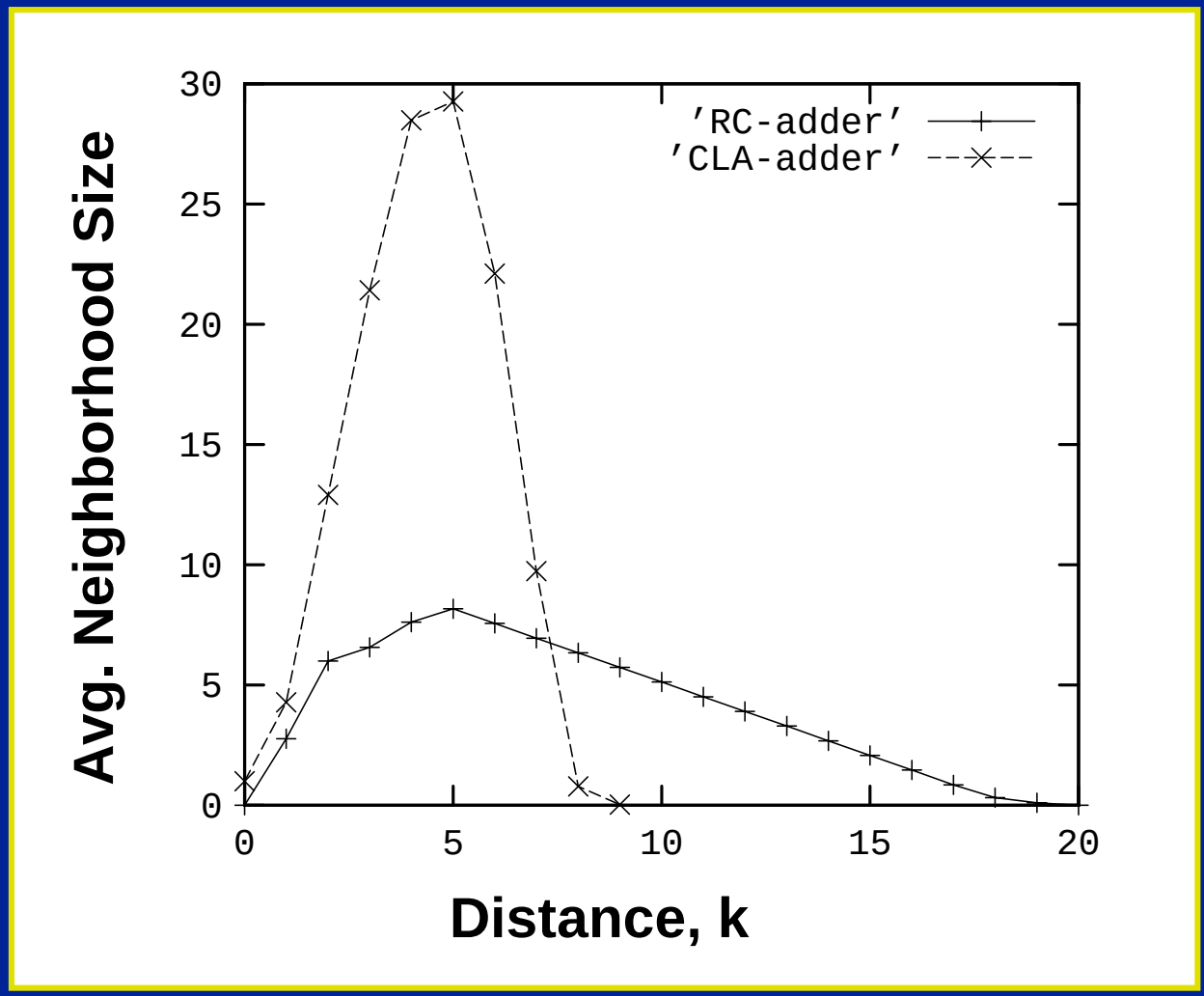
Ripple-carry



Carry-lookahead



# Distance Metric for Adders



# Application of Different Transforms

**Each transform tends to have its own effect on metric**

| Transform | mcnc-mapped | | | Average | | |
|---|---|---|---|---|---|---|
| | area | delay | cells | leng. | fanin | fanout |
| original[1] | 3452 | 71.6 | 1281 | 3.58 | 2.52 | 2.40 |
| fx[1] | 3190 | 69.5 | 1248 | 3.35 | 2.33 | 2.19 |
| resub[1] | 3090 | 69.7 | 1181 | 3.85 | 2.46 | 2.33 |
| speed_up[1] | 3438 | 54.5 | 1397 | 2.59 | 2.33 | 2.17 |
| speed_up[2] | 4672 | 41.6 | 2577 | 2.39 | 1.77 | 1.72 |

[1] map command used; [2] map -AF command used

Table 1. Results of the SIS-optimized circuit C5315.

| Transform | Distance, $k$ | | | | |
|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 |
| original[1] | 4.42 | 21.66 | 56.22 | 121.43 | 178.57 |
| fx[1] | 4.07 | 15.25 | 39.04 | 85.43 | 133.14 |
| resub[1] | 4.28 | 19.33 | 49.67 | 110.81 | 159.24 |
| speed_up[1] | 4.09 | 16.60 | 40.80 | 87.26 | 138.67 |
| speed_up[2] | 3.30 | 10.03 | 21.11 | 44.00 | 79.44 |

[1] map command used; [2] map -AF command used

Table 2. Distance metrics computed for the SIS-optimized circuits C5315.

# Experimental Observations

- A significant variability in distance metric is possible for different transforms
- Technology mapping could be a significant factor to the variability
- It is possible to improve distance metric along with other parameters (e.g. delay)

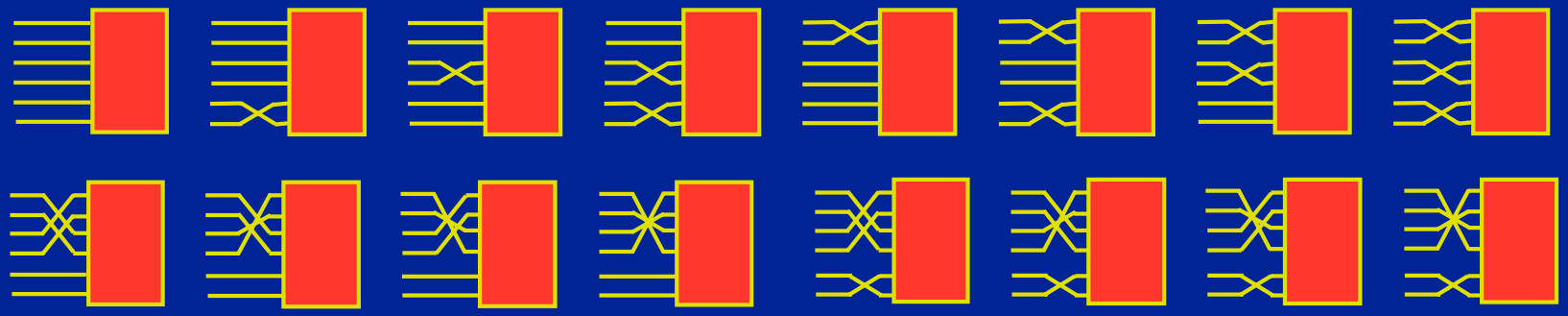
# Outline

- Motivation and approach
- Structural metrics
- **Logic transformations**
- Conclusions and future work

# Symmetry-Based Rewiring

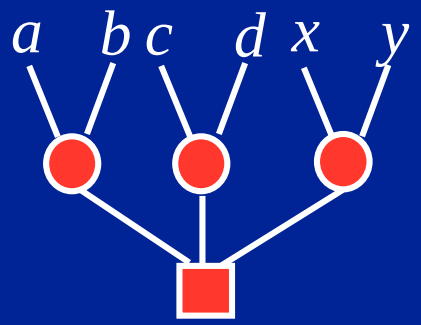
$f = abxy + cdxy$

$\langle\{\{a,b\}, \{c,d\}\}, \{x,y\}\rangle$



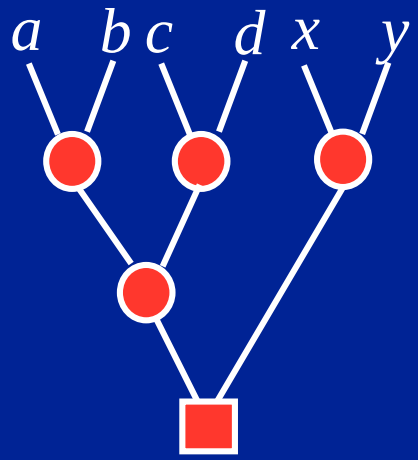
# Graphic Representation

$\langle \{a,b\}, \{c,d\}, \{x,y\} \rangle$




flat partition

$\langle \{\{a,b\}, \{c,d\}\}, \{x,y\} \rangle$

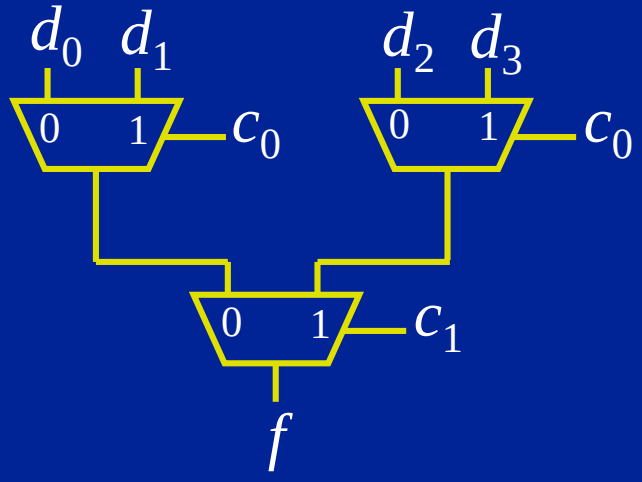


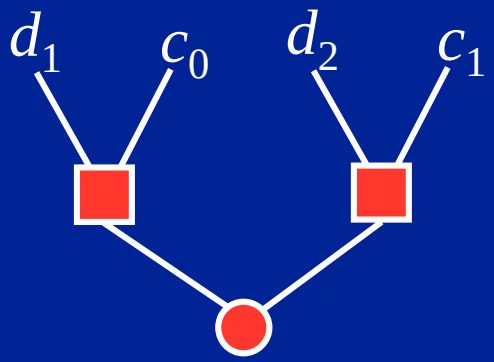

hierarchical partition

● means {}

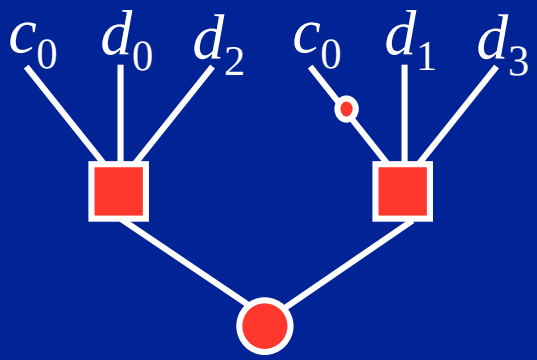
■ means ⟨⟩

# Multiplexer Symmetry



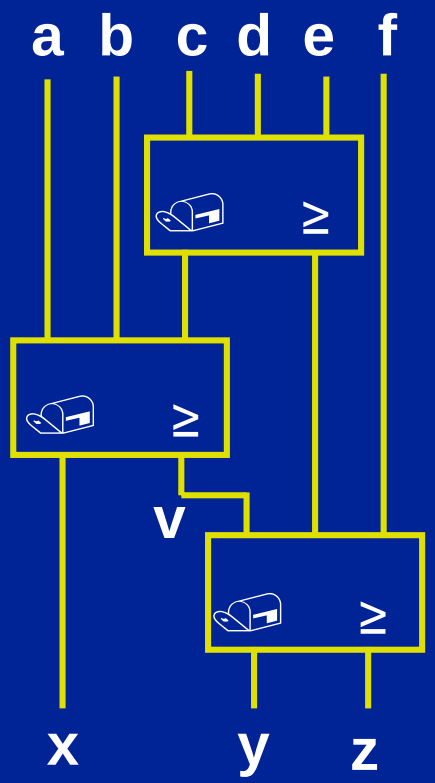




swap of ordered groups




multiplexer-like symmetry with phase assignments

# Simple Symmetry

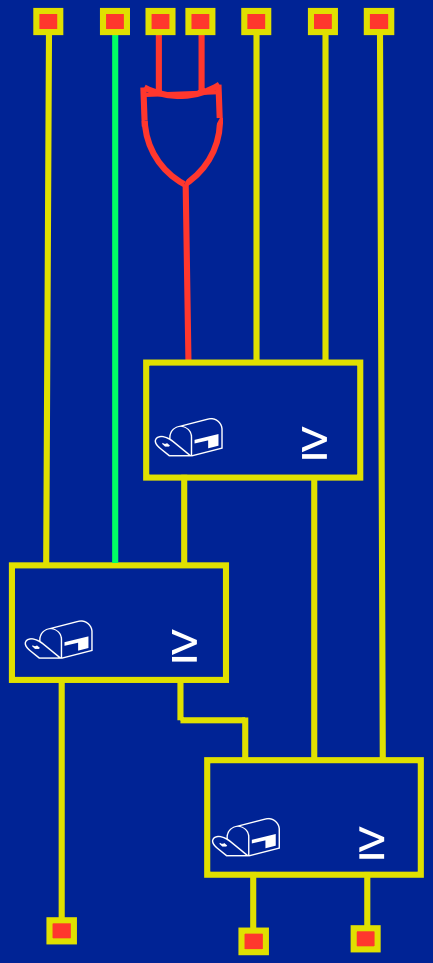



**For x:** $<\{a,b,c,d,e\}>$

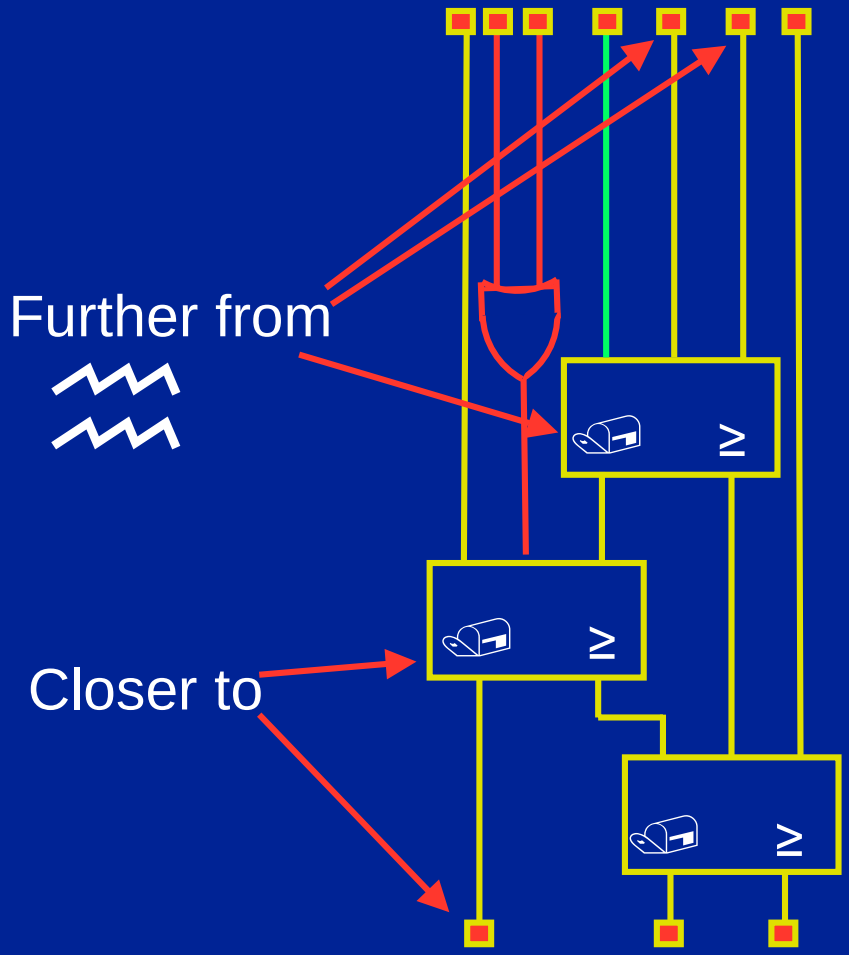
**For v:** $<\{a,b\},\{c,d,e\}>$

**For y, z:** $<\{a,b,c,d,e\},\{f\}>$

# Effect of a Swap on Metric



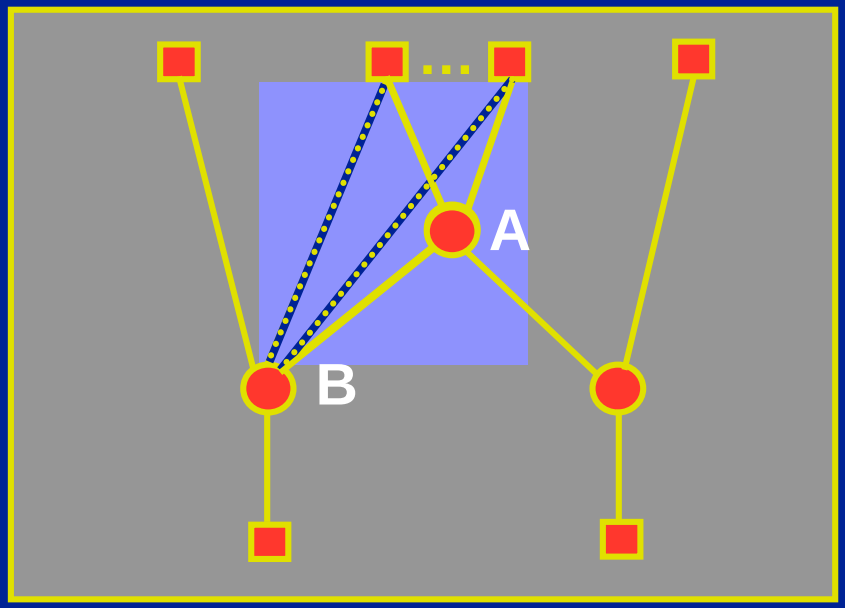
1:2.8 2:6.0 3:4.1 4:1.0




1:2.8 2:6.0 3:3.5 4:1.5

# Evaluation of Transformations

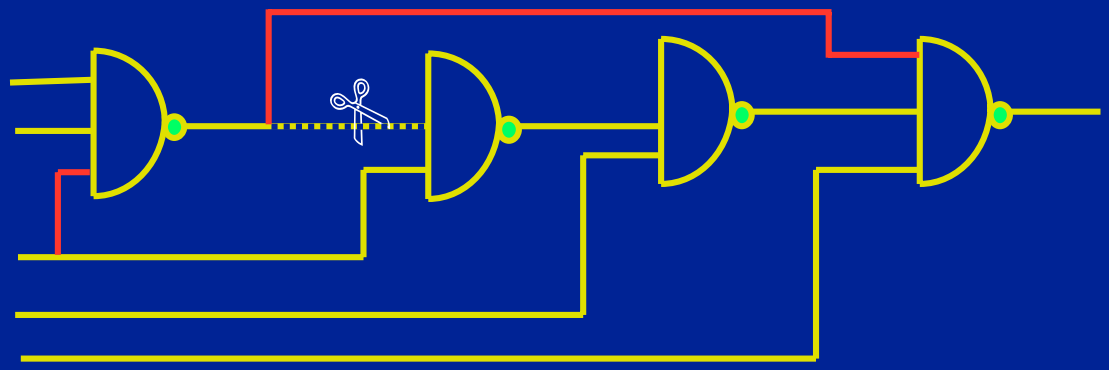
- Metric values depend on changes to paths going through A and B




- Consider immediate and extended neighborhoods of a change

# More General Local Restructuring

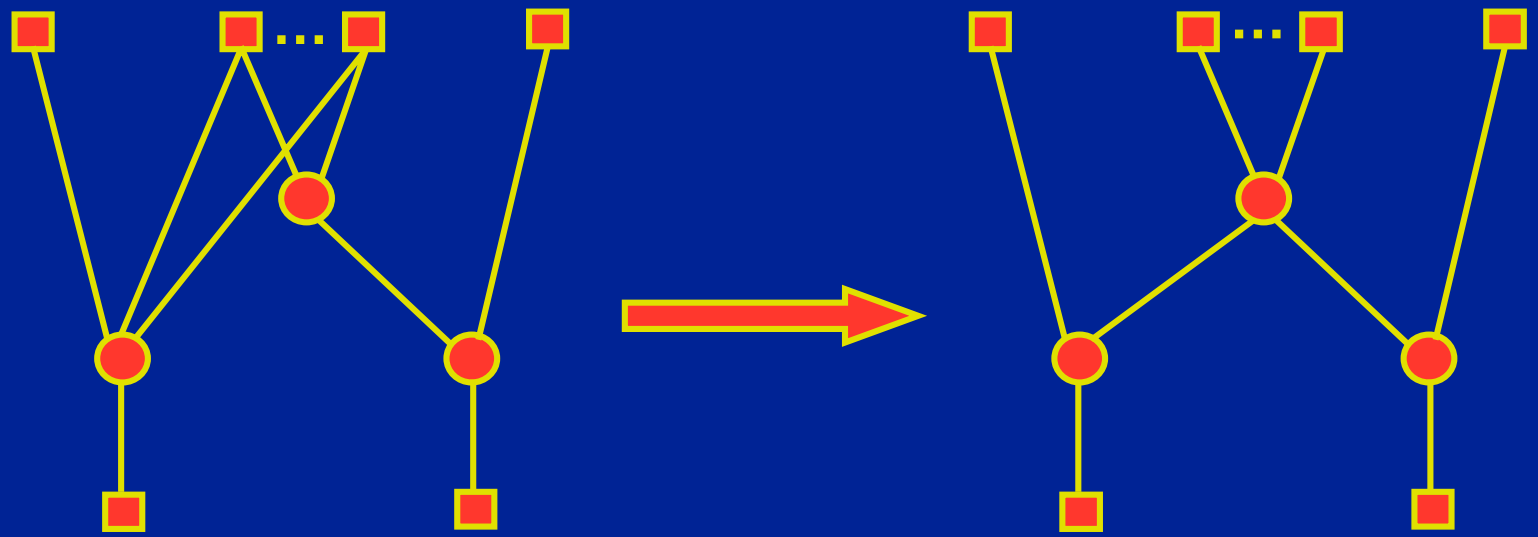
- Generic rewiring



- Resynthesis
  - re-decompose functional representation of circuit regions
  - disjoint decomposition is good for structure

# Aggressive Logic Synthesis Transforms

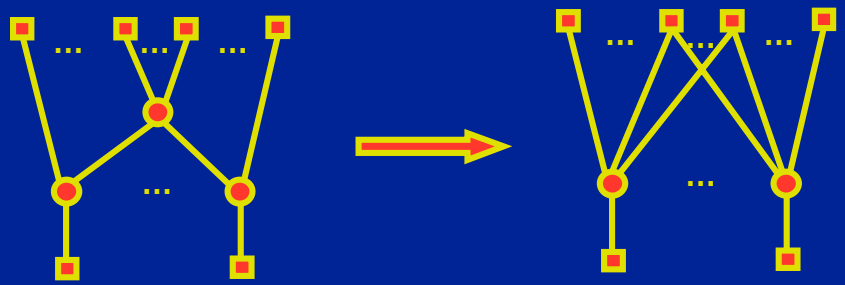
A resubstitution



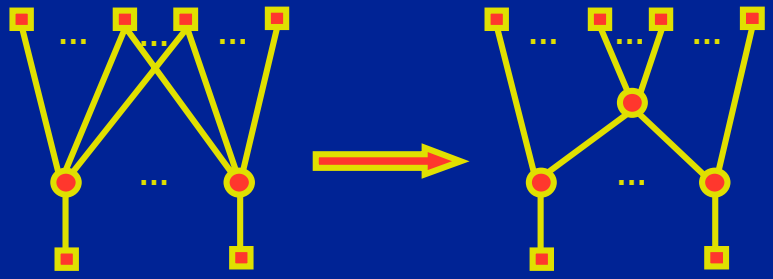
- Can be also described in terms of their rewiring patterns
- Their feasibility depends on global functional properties

# Variety of Transformations

**Collapsing**



**Extraction**

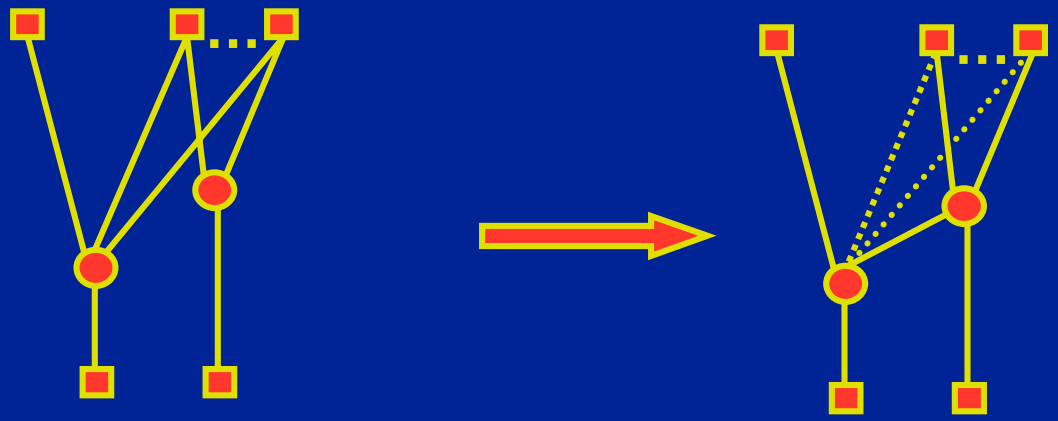


# Feasibility of Transformations

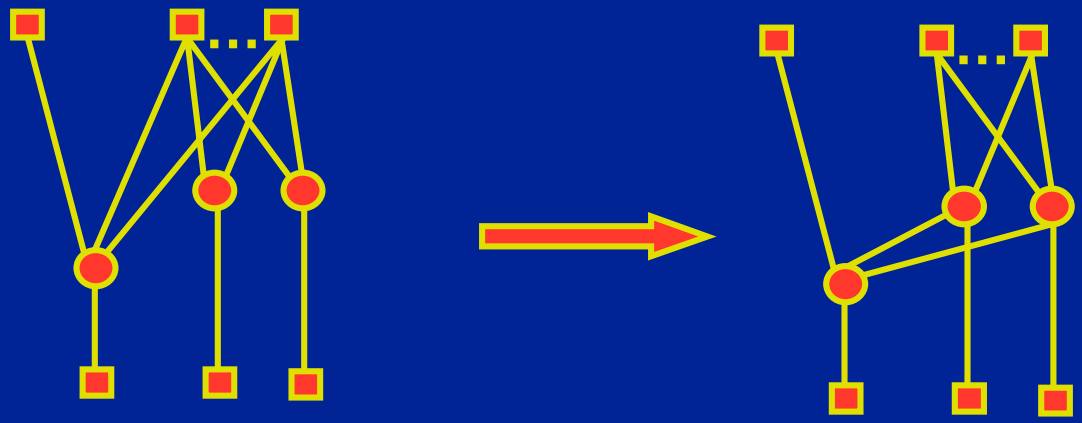
- Identification of a structural pattern in a circuit does imply feasibility of its transformation
- Boolean and algebraic methods have different domains of feasible transformations
- Boolean methods enable richer variety of transformations

# Resubstitution

**Algebraic resubstitution**



**Boolean 2-node resubstitution**



# Application of Boolean Resubstitution

**Original Circuit:**

**#Nodes 1832**

**#Levels 47**

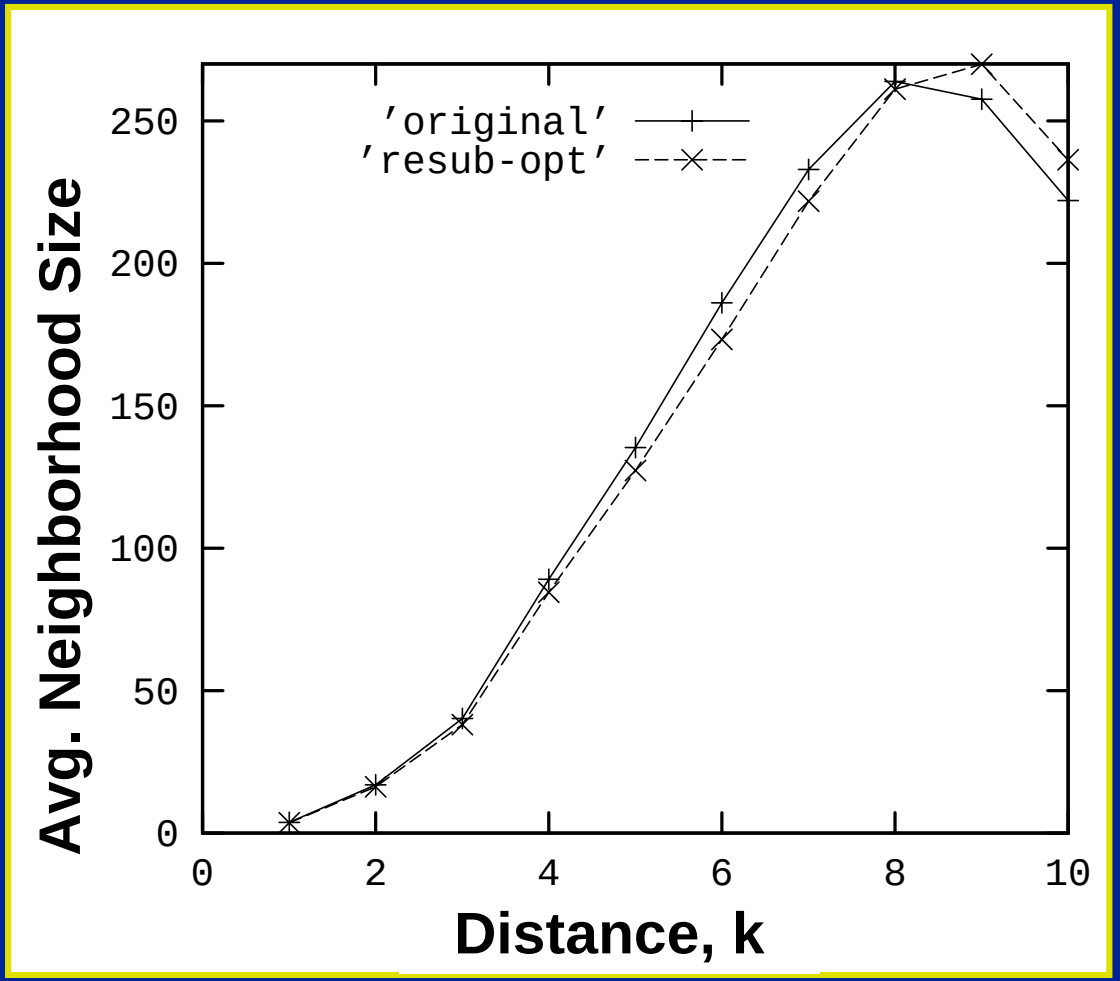
**#Wires 3787**

**Opt. Circuit:**

**#Nodes 1832**

**#Levels 50**

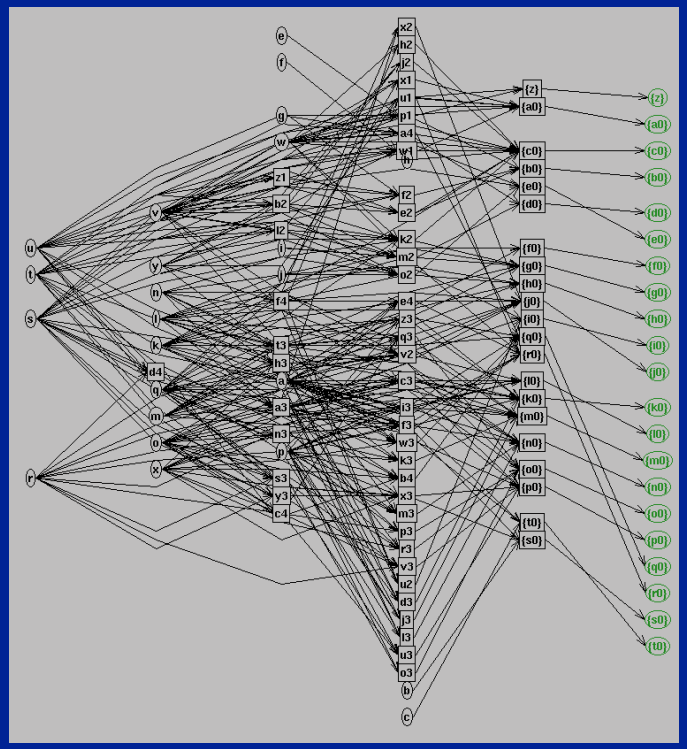
**#Wires 3707**



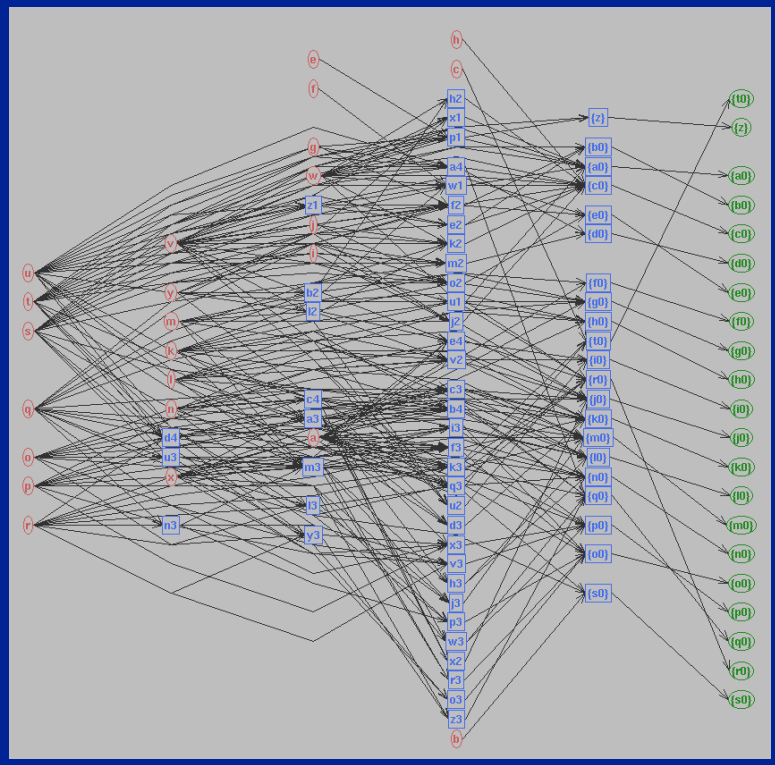

**Overall improved congestion observed after place&route**

# Boolean Resubstitution

**Example: 2-node resubstitution on a TI network**



**18 resubs**



**#Nodes 67;**

**Avg. Fanout 4.10, Fanin 4.28**

`1:6.3 2:28.5 3:31.2 4:18.9 5:5.5`

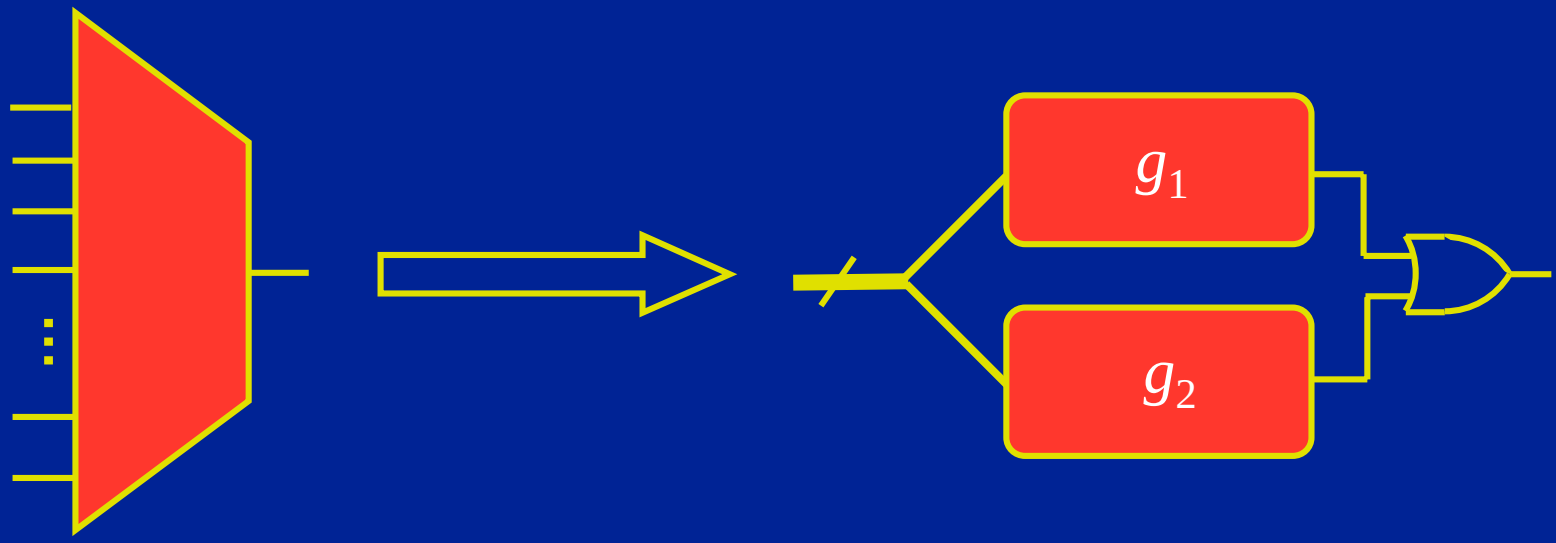
**#Nodes 64;**

**Avg. Fanout 4.01; Fanin 4.20**

`1:6.1 2:26.7 3:31.5 4:17.7 5:5.2`

# Leveraging Advances in CAD Software

**Solving MUX bi-decomposition for signals**




**What are *feasible* and *optimal* input connections to $g_1$ and $g_2$?**

# Use of BDDs

**Premise:** **Certain large combinatorial are efficiently manipulated with BDDs**

*Feasibility* *Optimality*

| MUX Width | | Complete Solution | | Best Partition of Inputs | |
|---|---|---|---|---|---|
| control | data | BDD size | CPU time sec | type | # solutions |
| 2 | 4 | 23 | 0.00 | <4,4> | 6 |
| 3 | 8 | 43 | 0.01 | <7,7> | 70 |
| 4 | 16 | 79 | 0.09 | <12,12> | 12870 |
| 5 | 32 | 147 | 1.35 | <21,21> | 6.0E8 |
| 6 | 64 | 279 | 20.56 | <38,38> | 1.8E18 |

# Outline

- Motivation and approach
- Structural metrics
- Logic transformations
- **Conclusions and future work**

# Conclusions

- Methods to capture global routability early in the design flow show promise
- Each logic transformation type tends to have its own structural impact
- Impact of transformations on structure could be evaluated analytically or statistically
- Transformations should be driven with a structural metric

# Future Work

- Other metrics: graph embedding, planarity, graph drawing
- Experiment with other technology independent optimizations as well as technology mapping
- New optimization techniques with richer set of feasible transformations should be developed
- Clustering properties of boolean functions
- IO assignment with logic synthesis
- Local congestion and detailed routing issues