Maximum Multiplicity Distribution (MMD)

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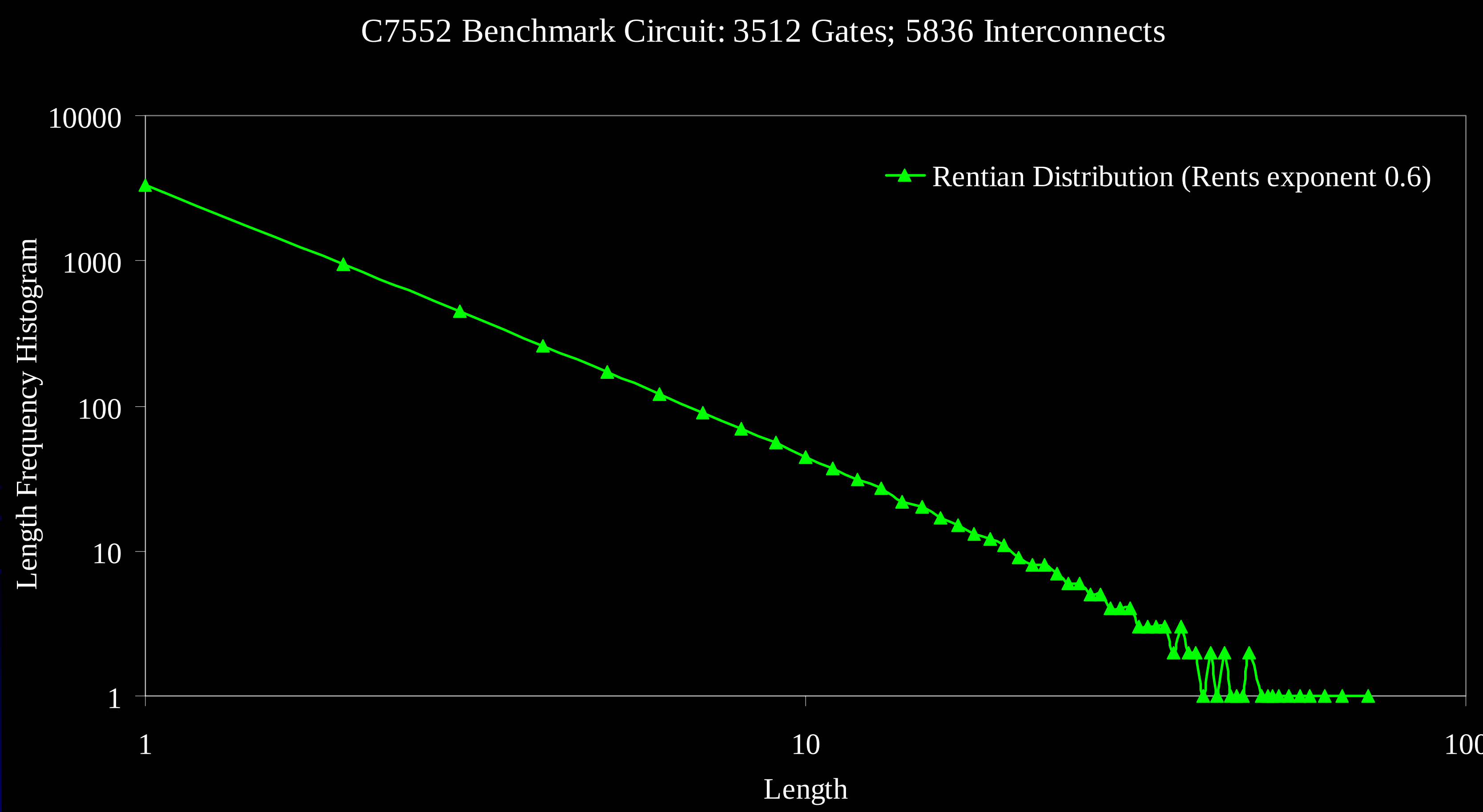
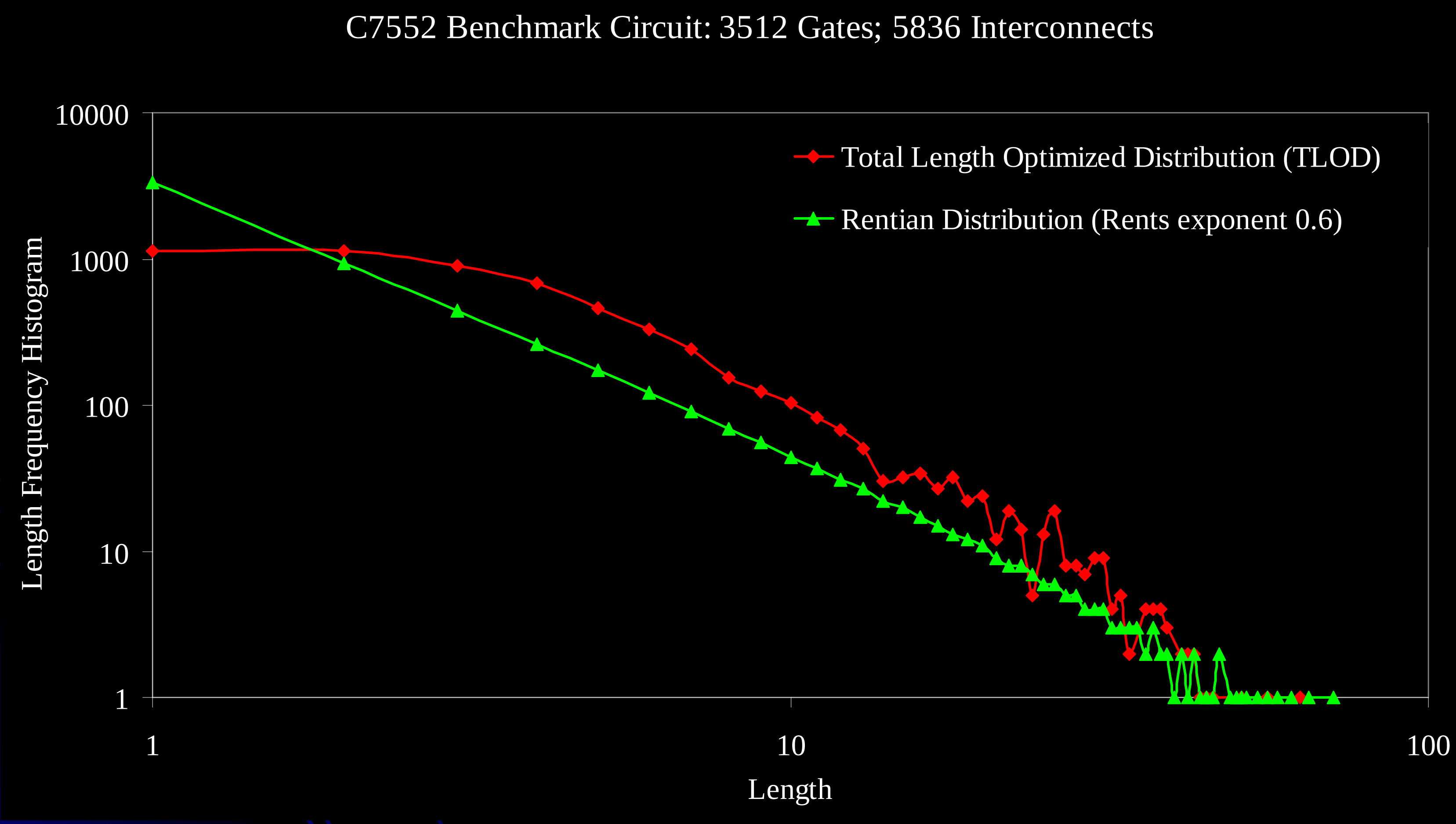
Rentian Length Distribution

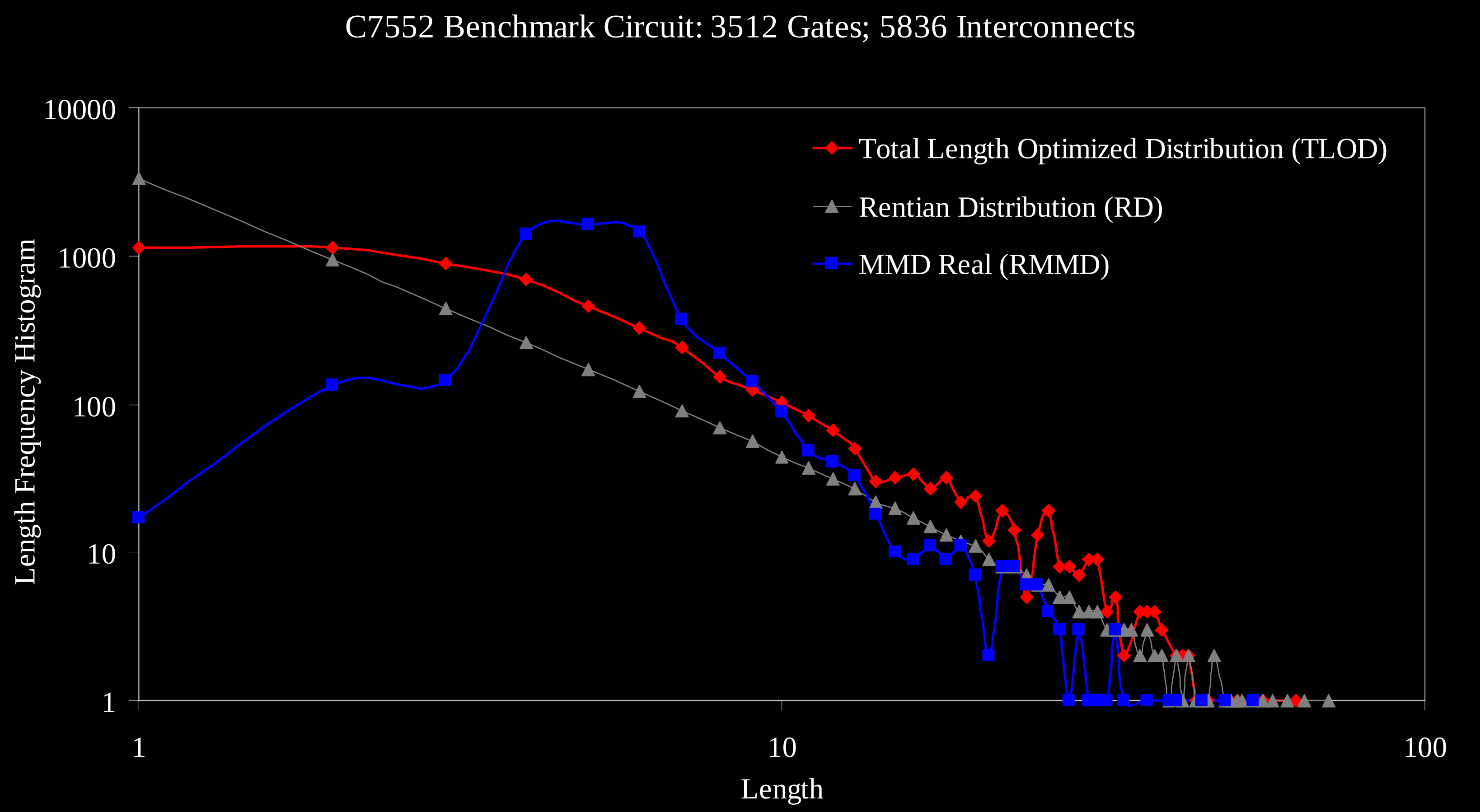


J. A. Davis, V. K. De, and J. D. Meindl, "A stochastic wire length distribution for gigascale integration (GSI) Part I: Derivation and Validation," IEEE Trans. Electron Devices, vol. 45, pp 580-589, March 1998.

Length Distribution



Length Distribution



Salient Properties of New Distribution

- Reduction in maximum length of interconnects
- Reduction in number of long interconnects
- Increases the available design space

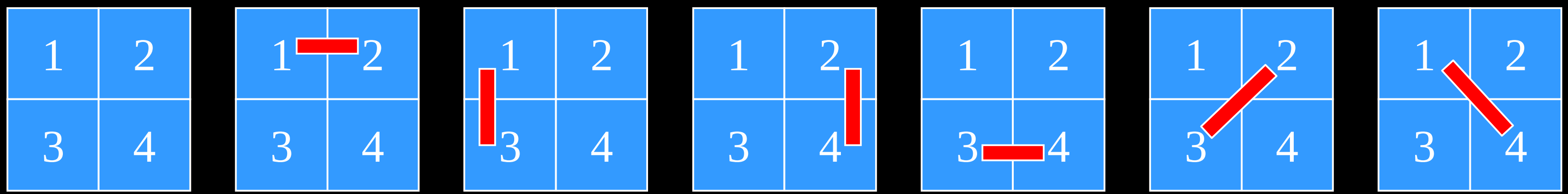
Outline

- *Multiplicity*
- Theoretical MMD
- Real MMD
- Impact on Global Interconnects
- Conclusion

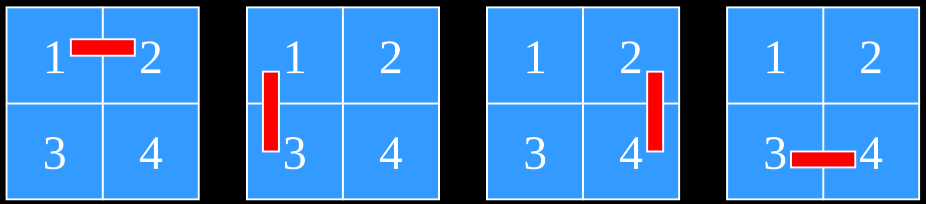
Multiplicity of Length Distribution

Total number of layout arrangements that have the same length distribution

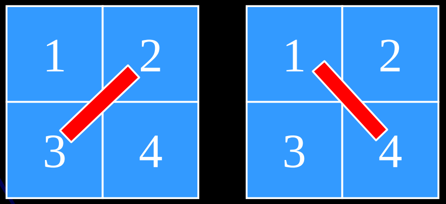
Interconnect Positions



- M[L]: Number of interconnect positions of length L in a layout
  - M[1]=4



  - M[2]=2



Interconnect Positions

- Density of interconnect states function M[L]

$1 \le L < \sqrt{N}: \qquad M[L] = \frac{L^3}{3} - 2L^2\sqrt{N} + \frac{1}{3}L(6N-1)$

$\sqrt{N} \le L < 2\sqrt{N} - 2: \qquad M[L] = -\frac{L^3}{3} + 2L^2\sqrt{N} - \frac{1}{3}L(12N-1) + \frac{2}{3}\sqrt{N}(4N-1)$

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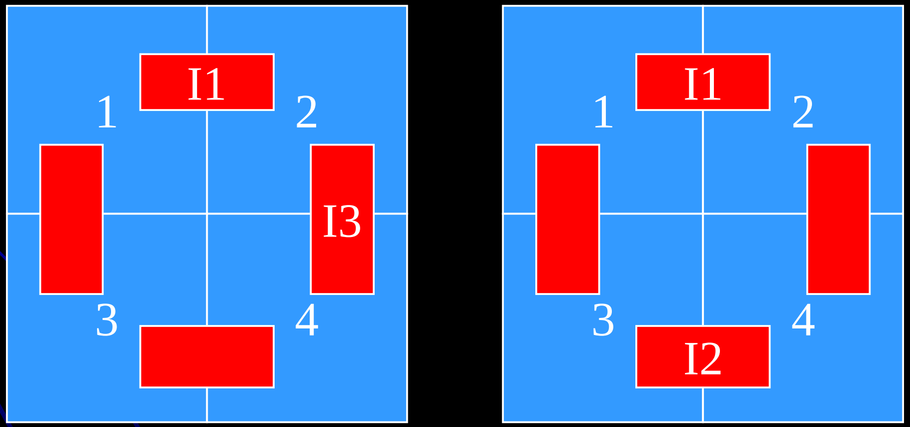
Multiplicity of Length Distribution

- Assumptions
  - Gates are arranged in a *homogeneous square layout array*
  - Interconnects are *independent*
  - Each interconnect is *distinct*

Independent Interconnects

- N[1] = 2

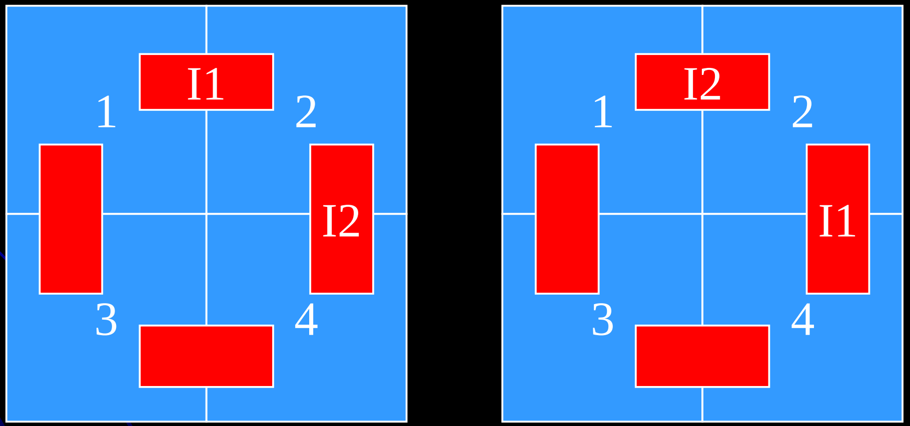
- Impossibilities Counted (Simple Calculations)!



Distinct Interconnects

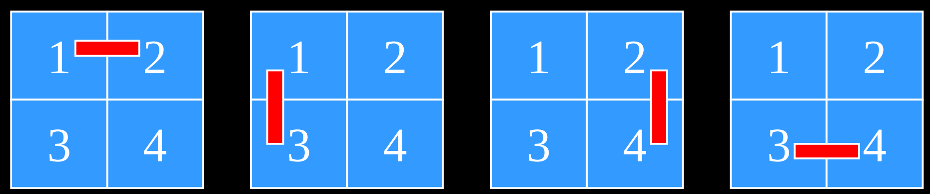
- N[1] = 2

- *Unique* arrangement should be counted!



Multiplicity of Length Distribution

- N[1]=2
- M[1]=4



- 4x3 {*M[1]x (M[1]-1)*} ways of arranging the 2 interconnects

$$\Omega_L = \prod_{I=0}^{N[L]-1} (M[L] - I)$$

- Multiplicity of interconnects of length L

$$\Omega_L = \frac{M[L]!}{(M[L] - N[L])!}$$

Multiplicity Calculation

- Multiplicity of interconnect length distribution

$$\Omega = \prod_{L=1}^{2\sqrt{N}-2} \frac{M[L]!}{(M[L]-N[L])!}$$

- Entropy

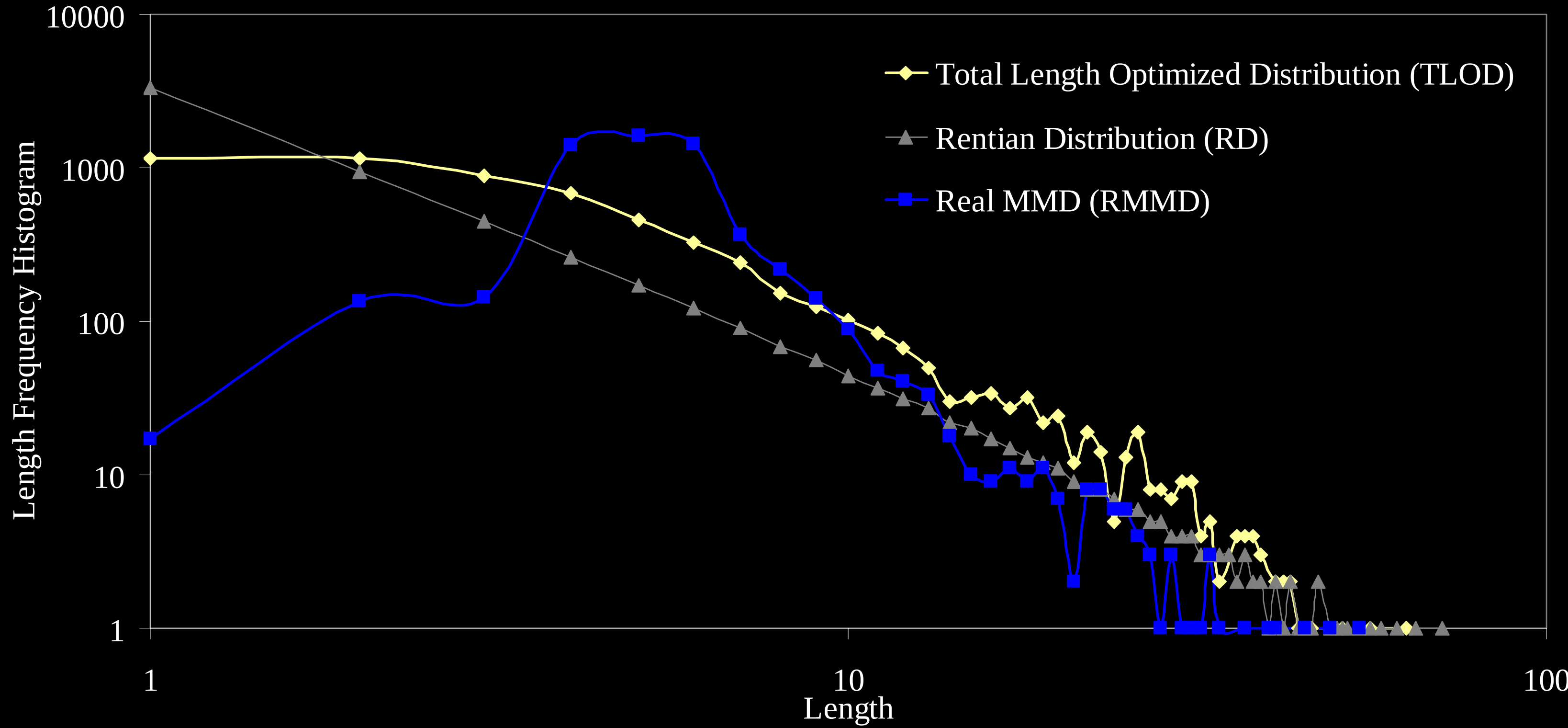
$$S = \sum_{L=1}^{L_{MAX}} \log(M[L]!) - \log((M[L]-N[L])!)$$

Length Distribution

C7552 Benchmark Circuit: 3512 Gates; 5836 Interconnects

Multiplicity of RD= $\mathbf{10^{20062}}$ < *Multiplicity of TLOD=* $\mathbf{10^{21858}}$ <

Multiplicity of RMMD= $\mathbf{10^{23084}}$



Outline

- Multiplicity
- *Theoretical MMD*
- Real MMD
- Impact on Global Interconnects
- Conclusion

MMD Problem Definition

- Find the values of N(L) such that S

$$S = \sum_{L=1}^{L_{MAX}} \log(M[L]!) - \log((M[L] - N[L])!)$$

is maximized under the following constraints

$$N_{Edges} = \sum_{L=1}^{L_{MAX}} N[L] \qquad L_{Total} = \sum_{L=1}^{L_{MAX}} L * N[L]$$

MMD Derivation

$$f_1 = \sum_{L=1}^{L_{MAX}} N[L] - N_{Edges} \quad (1)$$

$$f_2 = \sum_{L=1}^{L_{MAX}} L * N[L] - L_{Total} \quad (2)$$

$$\frac{\partial S}{\partial N[L]} + \alpha \frac{\partial f_1}{\partial N[L]} + \beta \frac{\partial f_2}{\partial N[L]} = 0 \quad (3)$$

$$\log(K!) = K \log(K) - K \quad (4)$$

$$\frac{\partial \log((M[L] - N[L])!)}{\partial N[L]} = -\log(M[L] - N[L]) \quad (5)$$

$$\frac{\partial \log((M[L] - N[L])!)}{\partial N[L]} + \alpha + \beta L = 0 \quad (6)$$

$$-\log(M[L] - N[L]) + \alpha + \beta L = 0 \quad (7)$$

$$N[L] = M[L] - e^{\alpha + \beta L} \quad (8)$$

$$N[L] = M[L] - e^{\alpha} e^{\beta L} \quad (9)$$

$$a = e^{\alpha} \qquad b = e^{\beta}$$

MMD Expression

$$N[L] = M[L] - a(b)^{L}$$

$1 \le L < \sqrt{N}$:

$$M[L] = \frac{L^3}{3} - 2L^2\sqrt{N} + \frac{1}{3}L(6N-1)$$

$\sqrt{N} \le L < 2\sqrt{N} - 2$:

$$M[L] = -\frac{L^3}{3} + 2L^2\sqrt{N} - \frac{1}{3}L(12N-1) + \frac{2}{3}\sqrt{N}(4N-1)$$

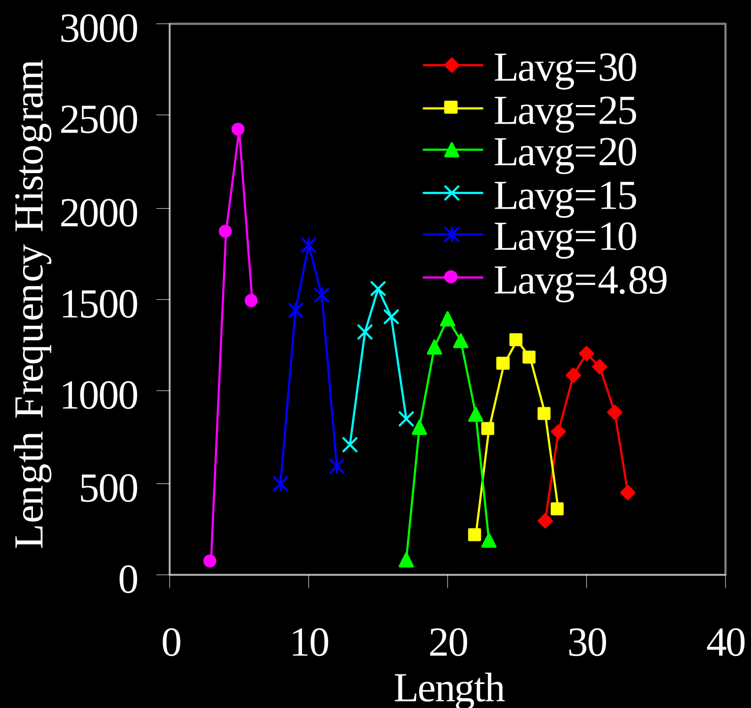
MMD Calculation

$$N[L] = Max(M[L] - a(b)^L, 0)$$

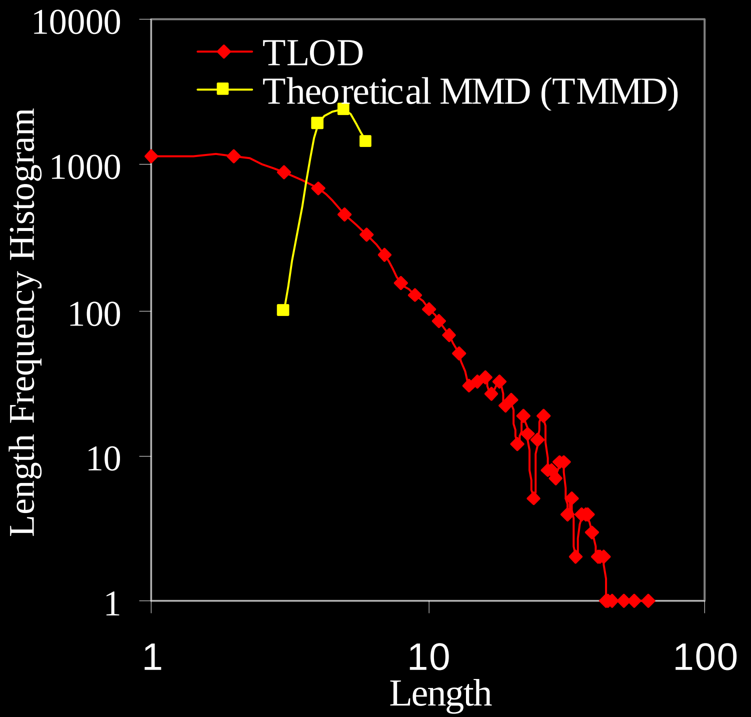
$$N_{Edges} = \sum_{L=1}^{L_{MAX}} Max(M[L] - a(b)^L, 0)$$

$$L_{Total} = \sum_{L=1}^{L_{MAX}} L * Max(M[L] - a(b)^L, 0)$$

MMD Calculation



MMD evolution for c7552 circuit with decreasing average length



TLOD and MMD for c7552 benchmark circuit with average length of 4.89

Outline

- Multiplicity
- Theoretical MMD
- *Real MMD*
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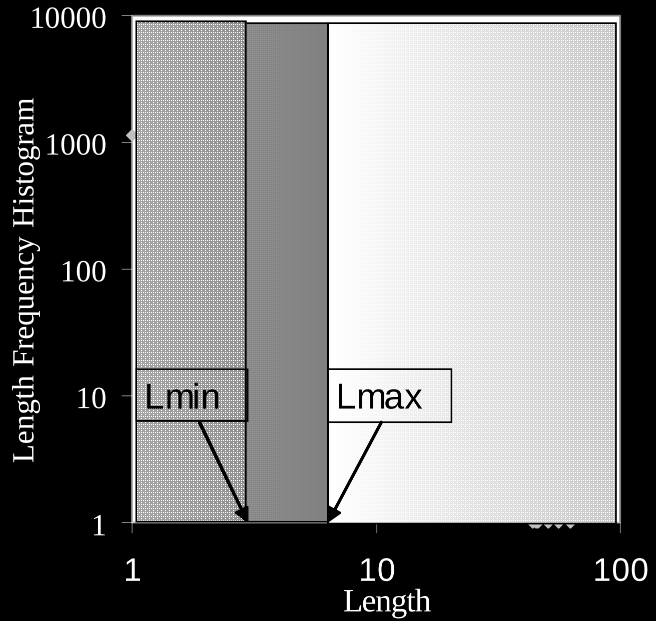
Real MMD

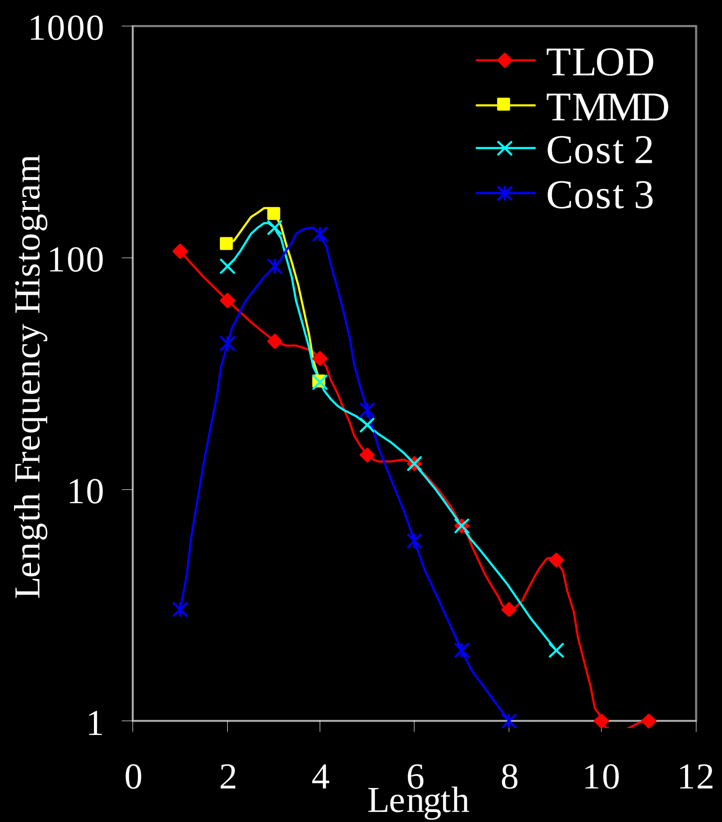
- Distribution Driven Placement

$$Cost = \sum W * \left| Nact[L] - Nreq[L] \right|$$



W values	Lact < Lmin	Lmin <= Lact <= Lmax	Lmax < Lact
Cost1	Lmin-Lact	Lact	Lact-Lmax
Cost2	Lmin-Lact	1	Lact-Lmax
Cost3	Lmin-Lact	0	Lact-Lmax
Cost4	Lact	Lact	Lact

Distribution Driven Placement



TLOD, Theoretical MMD, MMD-Distribution Matched (Real MMD) using cost function 2 and cost function 3

Circuit Name: C499	Cost1	Cost2	Cost3	Cost4
Cumulative % error	50.88	31.94	440.1	36.84
% Increase in total length	27.65	17.43	29.64	29.51

W values	Lact < Lmin	Lmin <= Lact <= Lmax	Lmax < Lact
Cost1	Lmin-Lact	Lact	Lact-Lmax
Cost2	Lmin-Lact	1	Lact-Lmax
Cost3	Lmin-Lact	0	Lact-Lmax
Cost4	Lact	Lact	Lact

Outline

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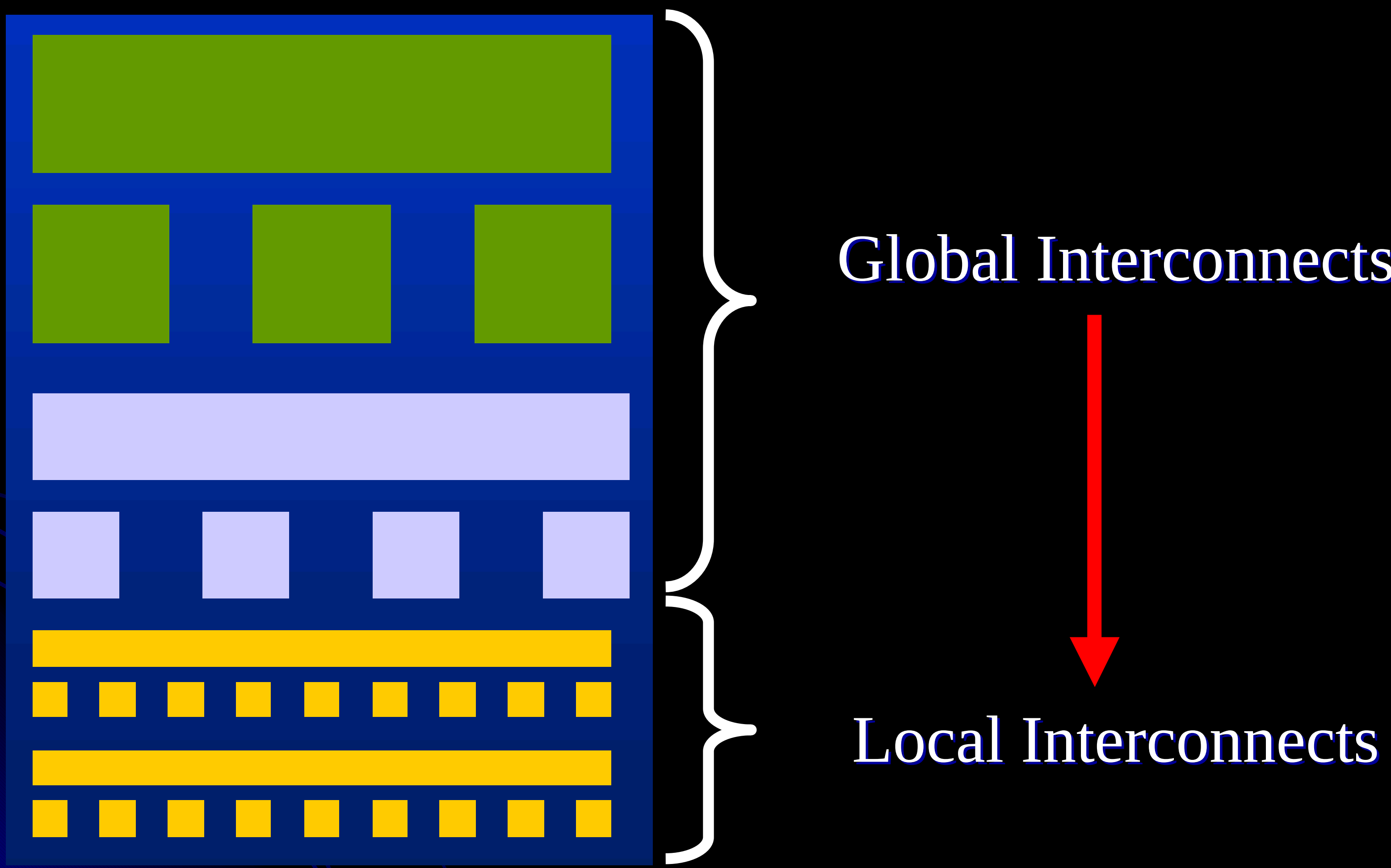
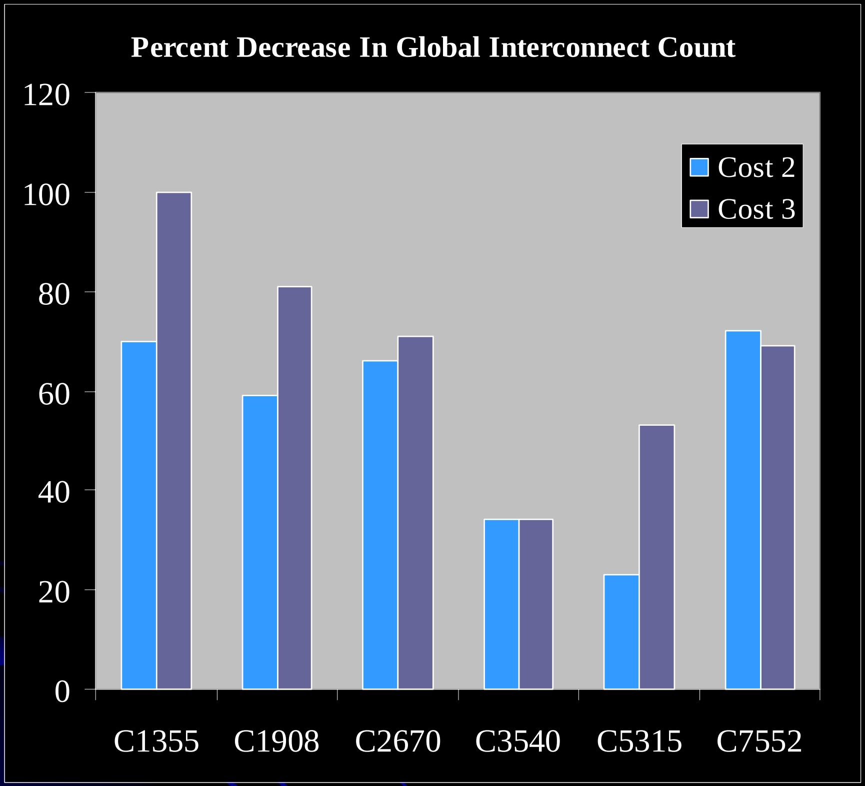
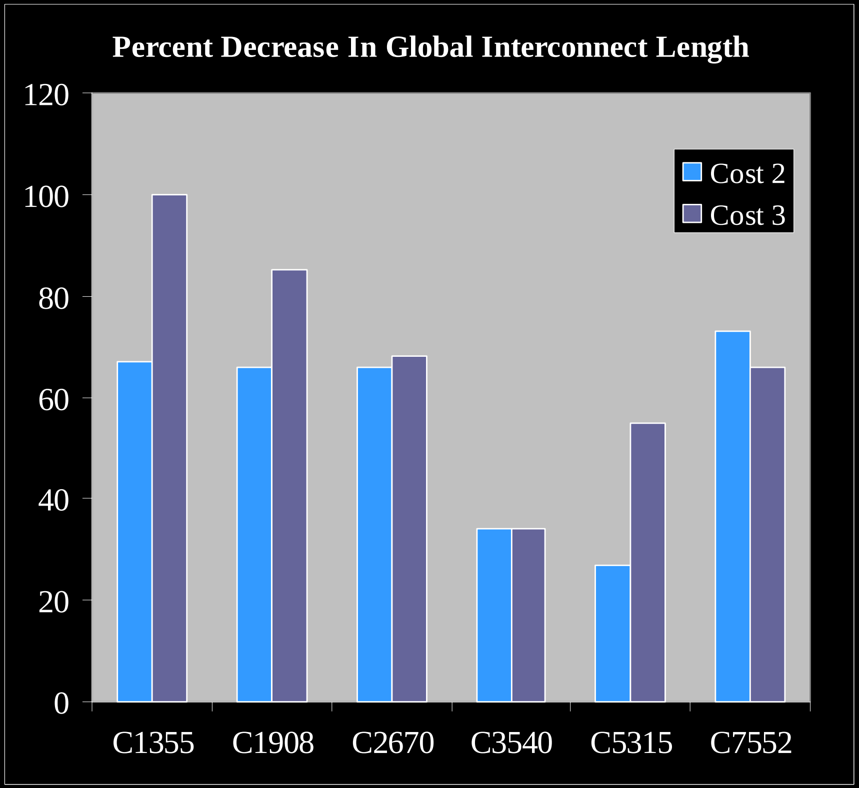
Multilevel Interconnect Architecture



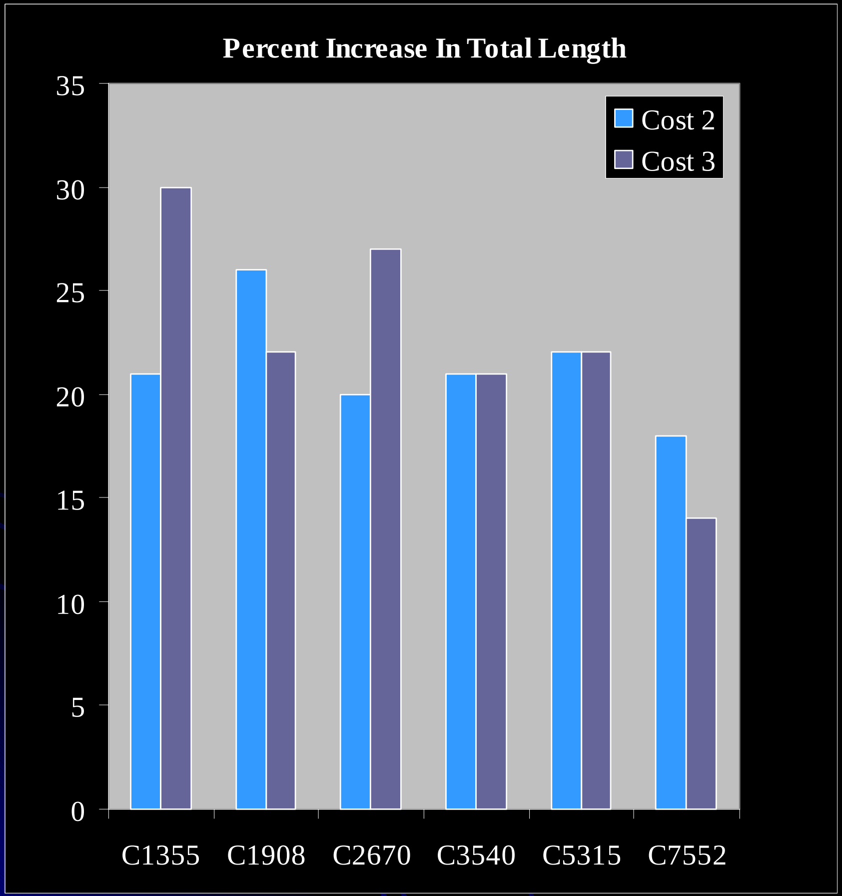
Global Interconnect





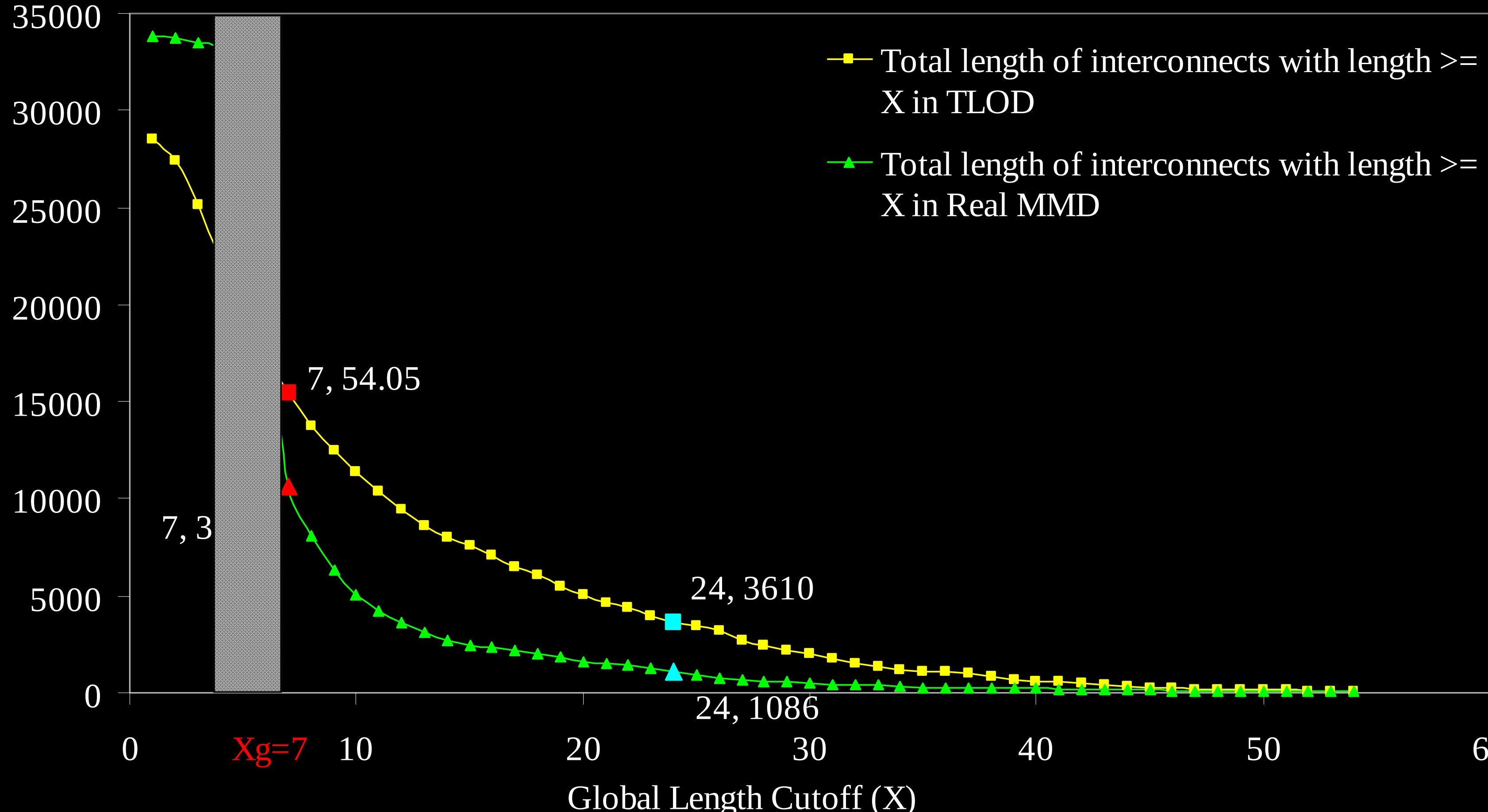
- Global Interconnect Cutoff = 0.2x L_{MAX}
- Global Interconnect Count - average improvement: 54% (Cost 2) vs 68% (Cost 3)
- Global Interconnect Length - average improvement: 55% (Cost 2) vs 68% (Cost 3)

Total Interconnect Length

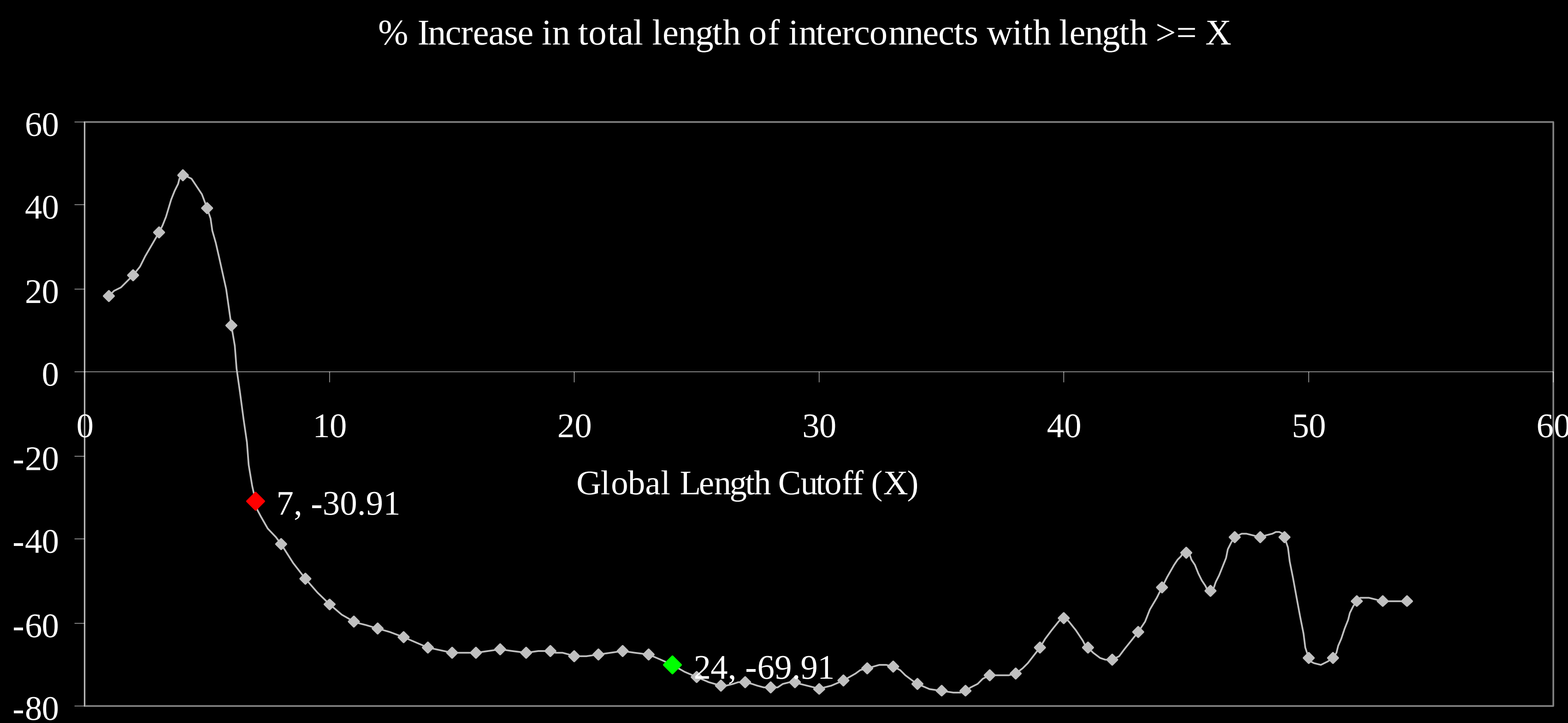


- Average increase in total length: 21% (cost 2) vs. 23% (cost 3)
- Interconnects with what length cause an increase in total length?
- What is the least length that we could use as global interconnect cutoff and see an improvement in global interconnect?

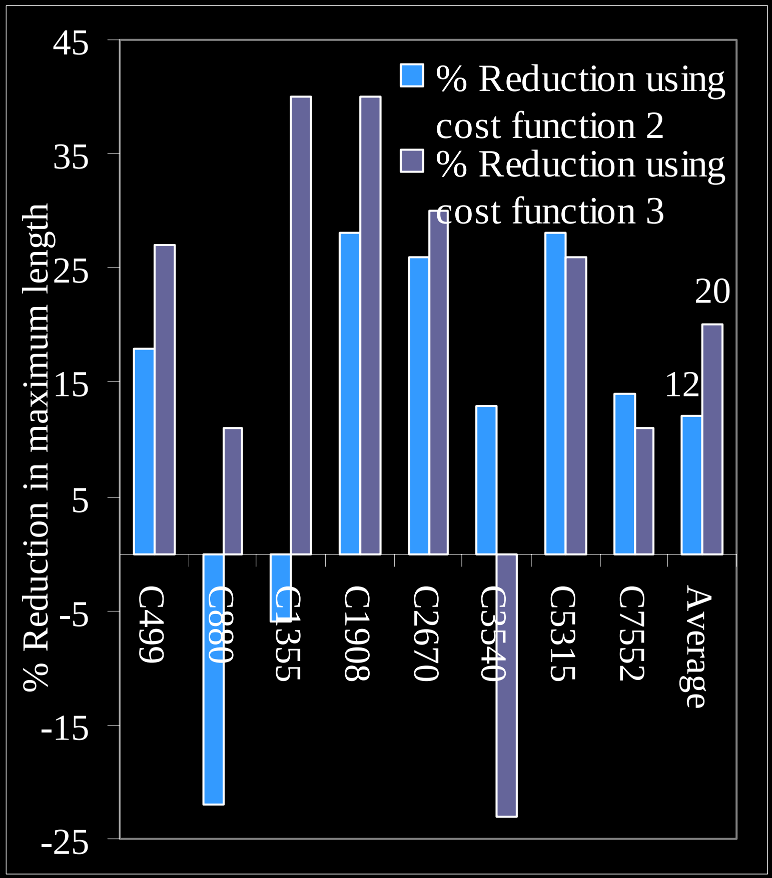
Global Interconnect Quality

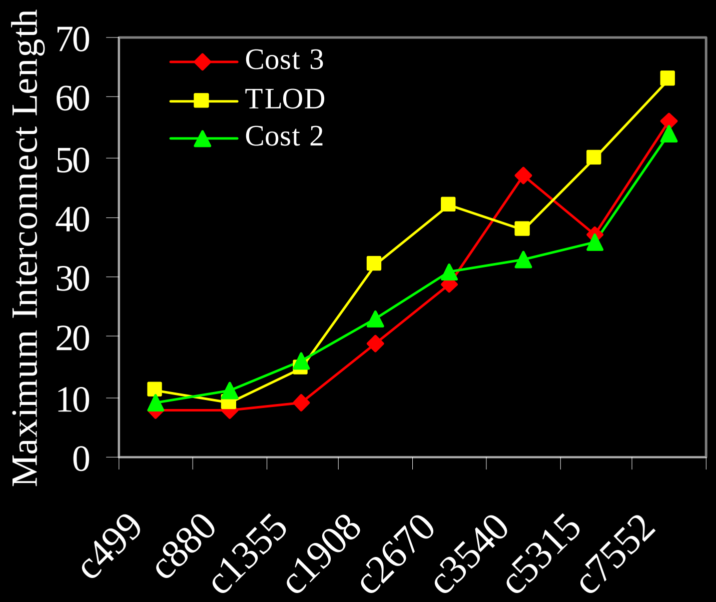


Global Interconnects



Global Interconnect Quality
Maximum Length





Maximum interconnect length resulting from cost function 2, cost function 3 and TLOD for various circuits.

Outline

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Conclusion

- New interconnect length distribution
- Reduction in
  - Number of long interconnects (55%)
  - Total length of long interconnects (55%)
  - Maximum length of long interconnects (12%)
- Increase in total interconnect length due to local interconnects
- Insight into Distribution driven Physical Design

Questions