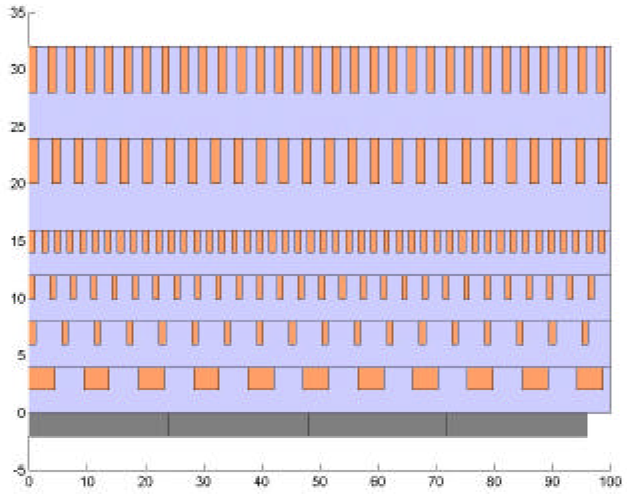
Wire Layer Geometry Optimization using Stochastic Wire Sampling

Raymond A. Wildman*, Joshua I. Kramer,
Daniel S. Weile, and Philip Christie
Electrical & Computer Engineering Department
University of Delaware

Introduction

Is it possible to optimize in-plane wire geometries (width, pitch) for individual netlists?



Previously we have attempted multi-objective (power, interconnect yield, clock rate) wire geometry optimization using Genetic Algorithms (GA)

BUT

Clock rate may be governed by just a few wires, leading to possible solution instability

We report on use of stochastic wire sampling in GA objective function

Outline

- Introduction
- Genetic Algorithms
- Pareto Optimization
- Stochastic Cycle Time Analysis
- Results
- Conclusions

Genetic Algorithms: Introduction

- GAs are optimization algorithms based on Darwin's Theory of Evolution.
- Advantages of GAs: They
  - Tend to find global or strong local optima
  - Work without derivatives
  - Work with both continuous and discrete variables
  - Are simple to implement, pliable, and extensible.
- GAs have designed of the turbines of the Boeing 777 engine, written music, played the stock market, and designed countless other devices in all disciplines of engineering.

Genetic Algorithms: Overview

- Work with coded forms of potential solutions called chromosomes.
- Work with an entire population of chromosomes instead of a single candidate solution.
- Chromosomes are evaluated and given a fitness value by an objective function
- Iteratively performs 3 operators on the population:
  - Selection
  - Crossover
  - Mutation

UNIVERSITY OF DELAWARE

Coding and Initialization

- GAs can work with many different types of codings, but the most common is binary.

0110 → 6

Real Decoding:

$$\frac{6}{2^4-1}\left(p_{max}-p_{min}\right)$$

Database Decoding:

$$\begin{pmatrix} 0 & 1 & \cdots & 15 \\ \downarrow & \downarrow & \cdots & \downarrow \\ 50 & 60 & \cdots & 75 \end{pmatrix}$$

- Different design parameters are strung together to create a chromosome that fully describes a design.
- A population is created by randomly initializing N chromosomes.

Selection

- Responsible for implementing “survival of the fittest,” and thus for convergence.
- Many types, but here binary tournament selection is used.
  - Two members chosen at random from population
  - Better member saved in “new population” for further genetic manipulation

Crossover and Mutation

- Crossover hybridizes chromosomes with given probability
  - Random crossover point is chosen
  - Chromosomes exchange right halves

```
010010|011      →      010010|110
101110|110      →      101110|011
```

- Mutation randomly perturbs chromosomes with a given probability

```
010010011      →      010000011
```

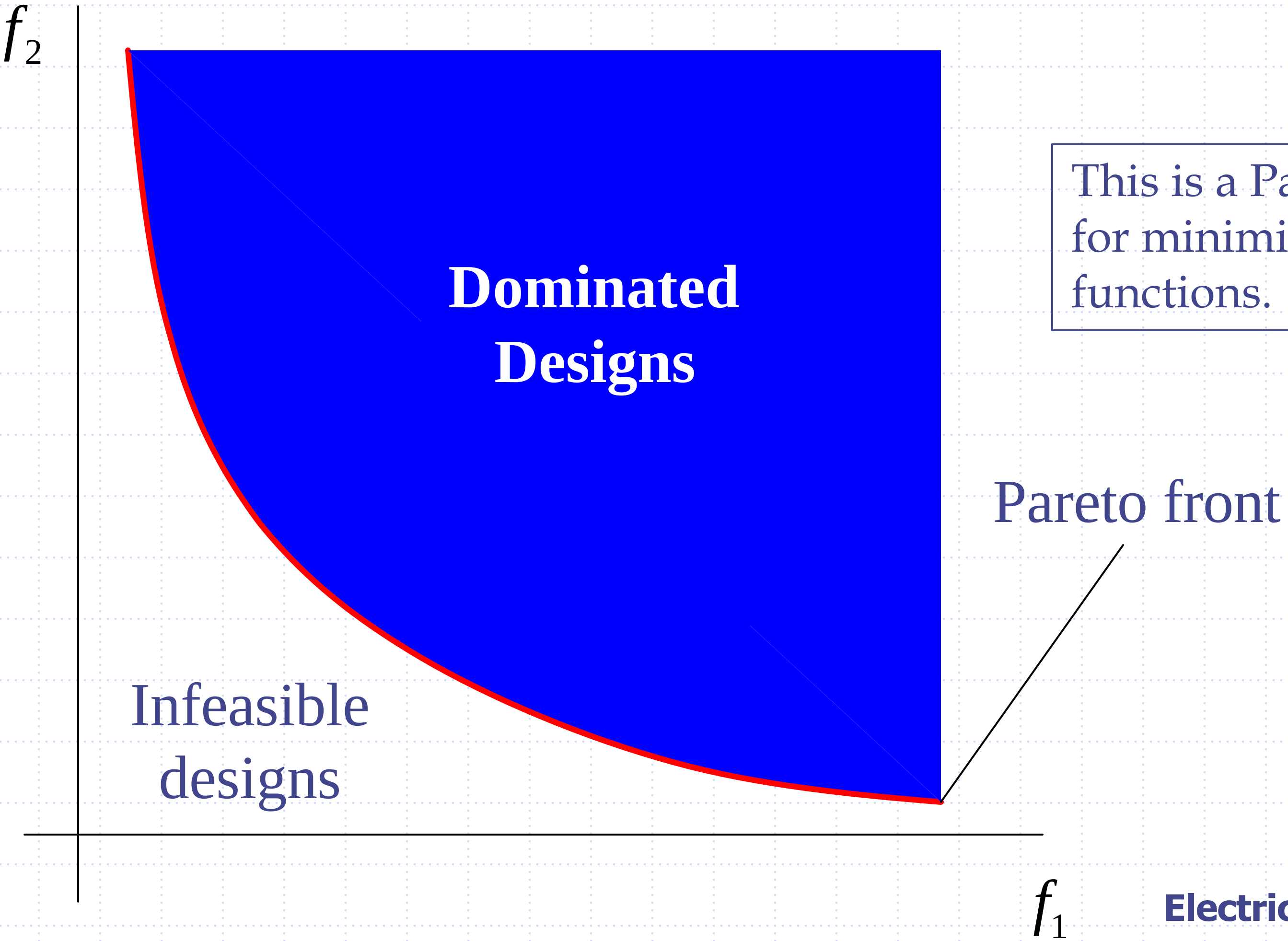
Crossover is more important than mutation, as it manipulates genes that have survived.

UNIVERSITY OF DELAWARE

Pareto Optimization

- Pareto optimization allows us to choose from a set of the best designs, effectively reducing an engineering problem to a management problem.
- A design is said to be dominated if there exists another design which is as good or better in all respects.
- A design is said to be nondominated, efficient or Pareto optimal if it is not dominated.
- The Pareto front or Pareto optimal set is the set of all nondominated designs in a given search space.

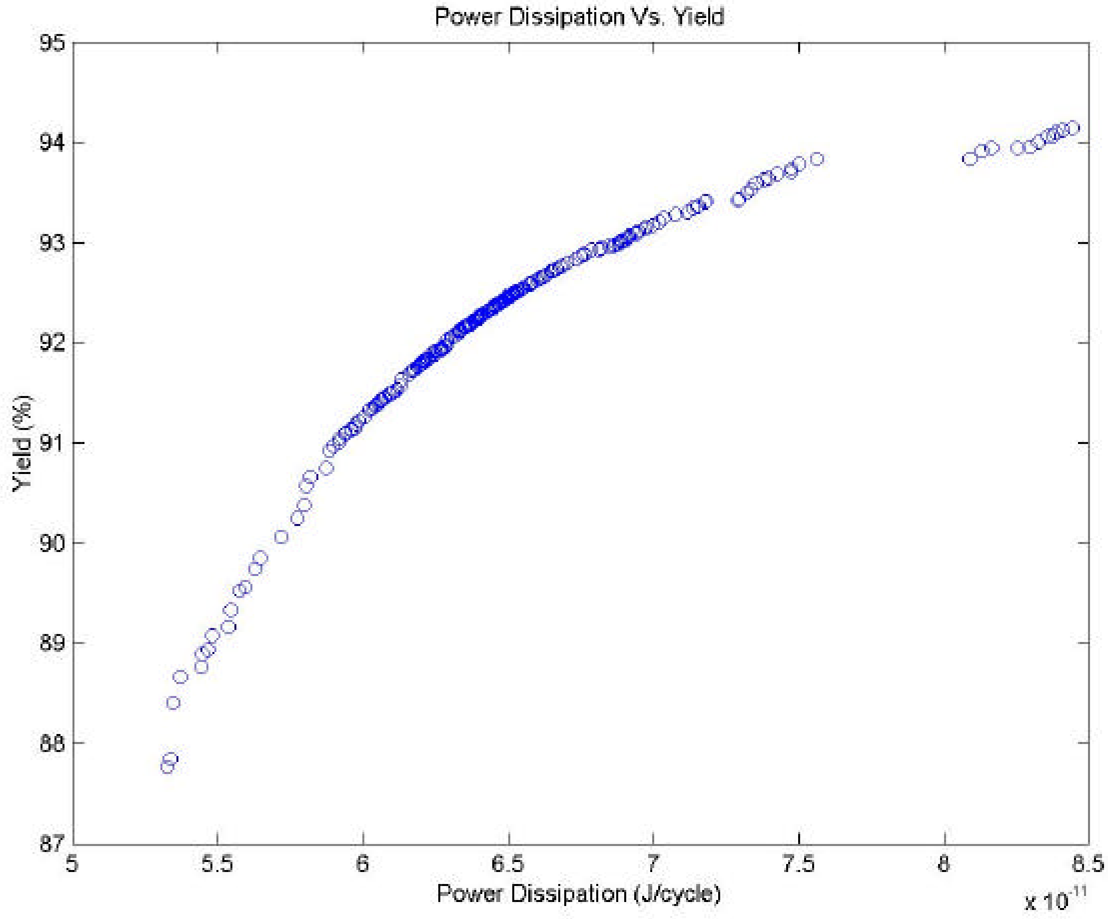
The Pareto Front



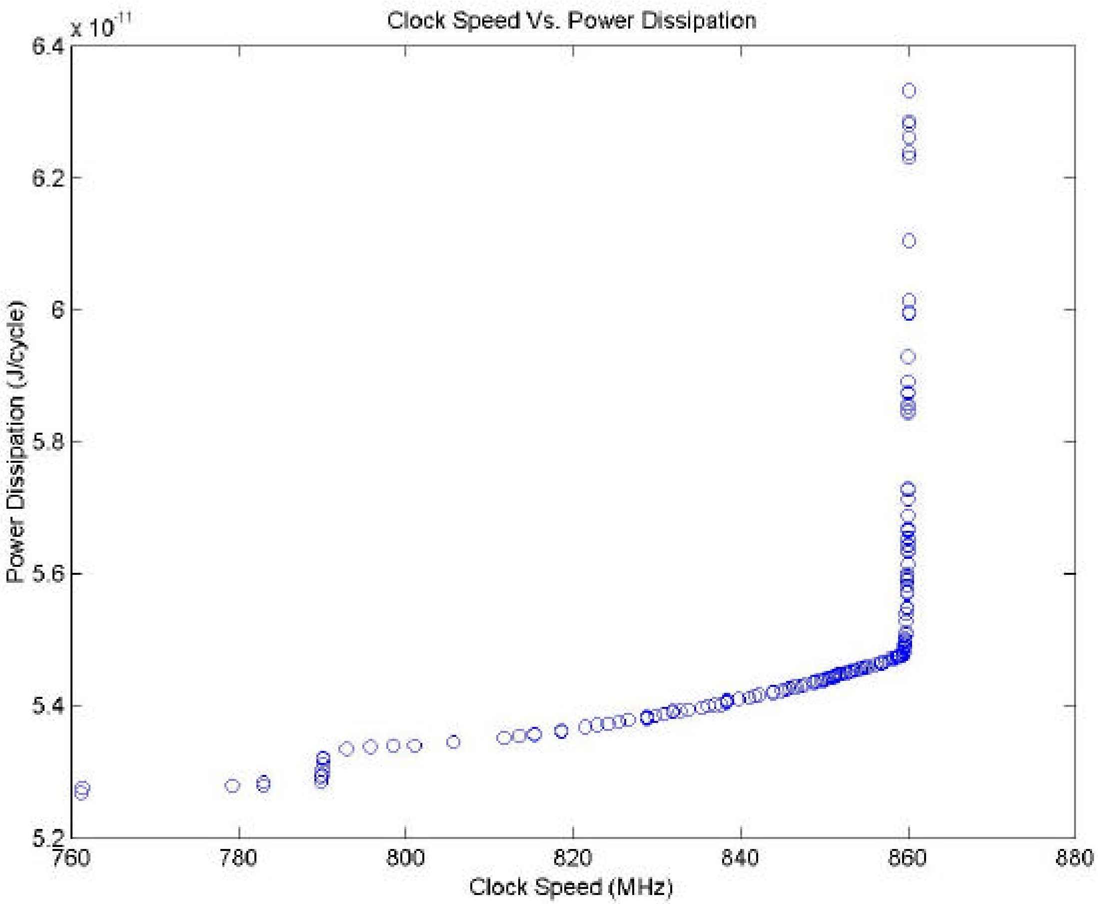
This is a Pareto front for minimizing two functions.

Electrical & Computer Engineering

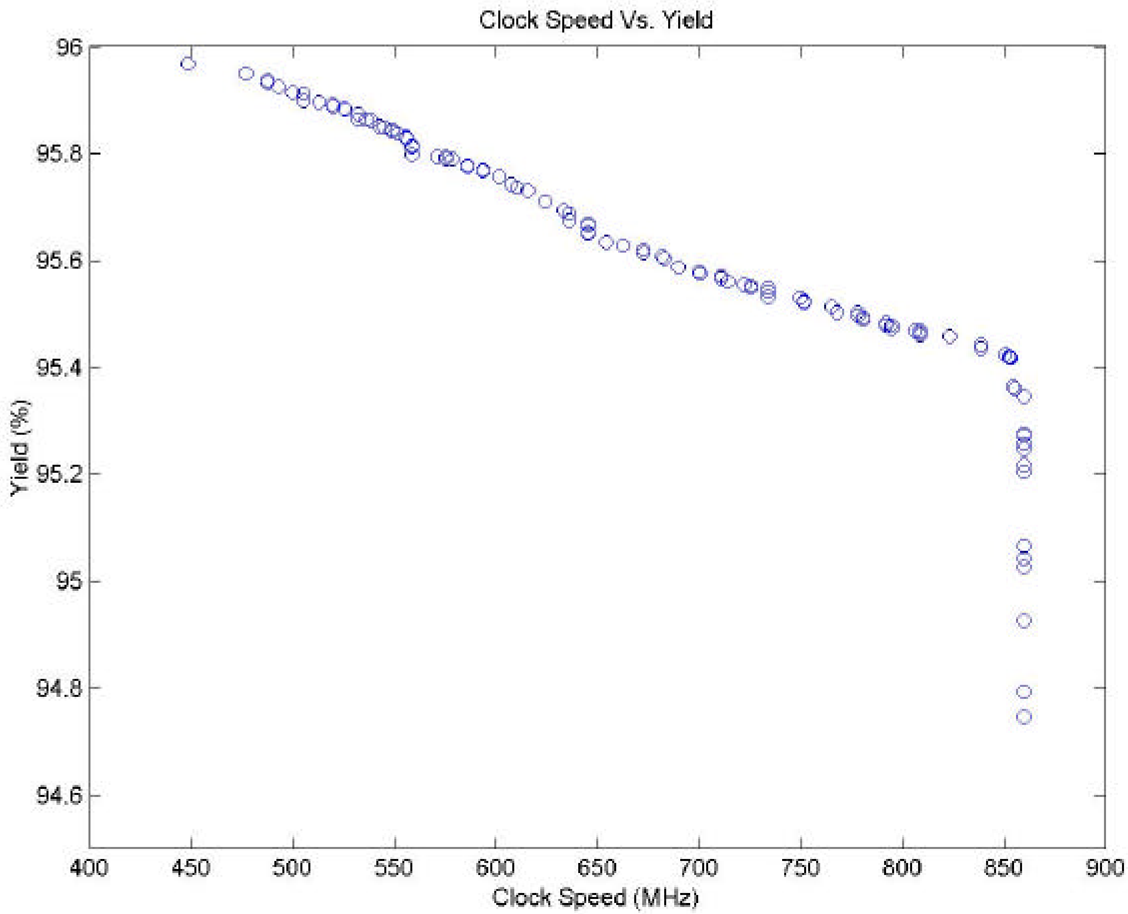
Previous Pareto Work



Previous Pareto Work



Previous Pareto Work



Clock Speed Axis

- The Problem:
  - Previous cycle time estimates used only wires of maximum and average length
  - GA only optimized the layer containing the wire of maximum or average length
  - Using the average wire could be a good estimate if the chip is device limited
  - In the future, larger chips will be limited by the longer wires required to connect the devices
- The Solution:
  - Use a stochastic technique to incorporate all wiring layers in the clock speed estimation

Stochastic Cycle Time Model

- Cycle time of combinational logic between two latches estimated using sum of local, global, setup, and latch delays
- Setup Delay: Time needed for signal to stabilize
- Latch Delay: Signal transition time through a latch
- Global Delay: Delay due to very long wires
- Local Delay:
  - Sample the wire length distribution
  - Delay is calculated through 25 layers of logic gates that are connected by the sampled wires.

Wire Length Distribution Sampling

- Choose 25 wire lengths
  - Ex: 3 44 1 2 1 2 5 3 2 2 2 2 16 2 2 1 3 1 2 3 4 2 43 2 2
    - Avg. Length = 6.2, max = 44
  - Ex: 2 1 12 8 10 63 1 1 3 23 2 30 8 1 2 16 2 18 1 1 2 1 2 1 38
    - Avg. Length = 10, max = 63

Clock Speed Objective Function

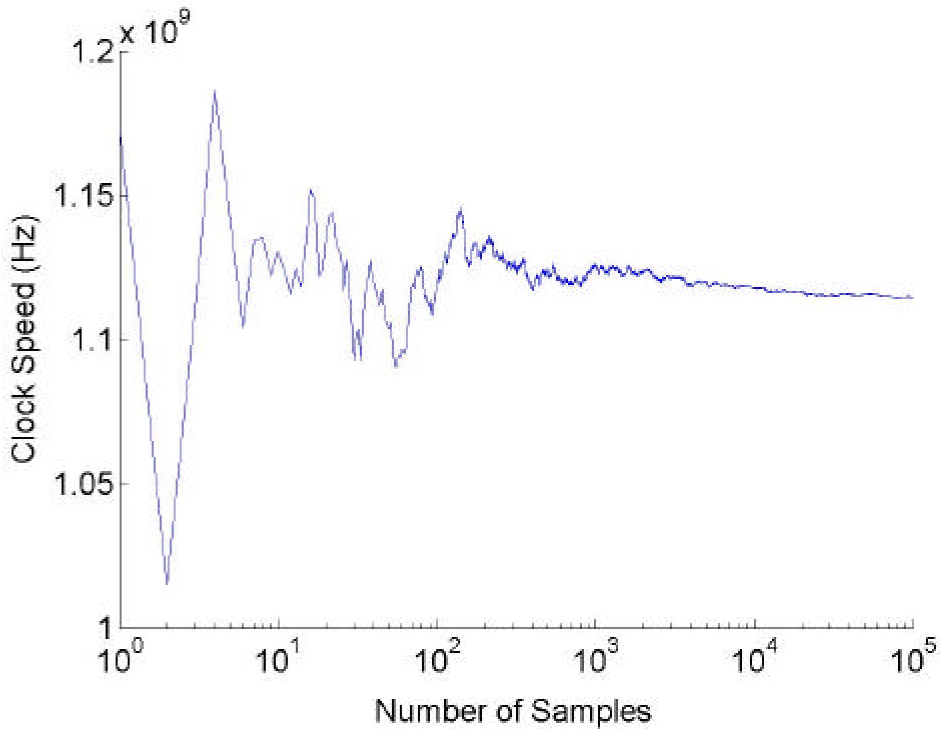
- Problem:
  - Each design will not evaluate the same for each sampling
  - Most optimization algorithms will not function in the presence of a noisy objective function
- Solution:
  - Average N_{samp} samples of 25 wires

Three Definitions of Sampling

- The cycle time model calculates local delays by sampling the wire length distribution for 25 wires
- N_{samp} samples of groups of 25 wires are averaged to estimate the clock speed
- The GA evaluates a population or sample of designs
  - A design is a combination of wire widths and spacings
  - The GA re-evaluates all designs each generation

Choosing N_{samp}

- Takes many samples to converge
- Too computationally expensive
- How many samples can be used so that the GA will converge?



UNIVERSITY OF DELAWARE

Results: GA Parameters

- Binary Chromosome length 72 bits
  - 6 layered chip
  - 6 bits for each width and spacing
- Wire widths varied from 1 to 5 μm
- Wire spacing varied from .2 to 5 μm
- Vertical parameters
  - Height in layers 1-4 was fixed at 2 μm
  - Pitch in layers 1-4 was fixed at 4 μm
  - Height in layers 5 and 6 was fixed at 4 μm
  - Pitch in layers 5 and 6 was fixed at 8 μm
- Probability of crossover was 85%
- Probability of mutation was .5%
- Population size was 100

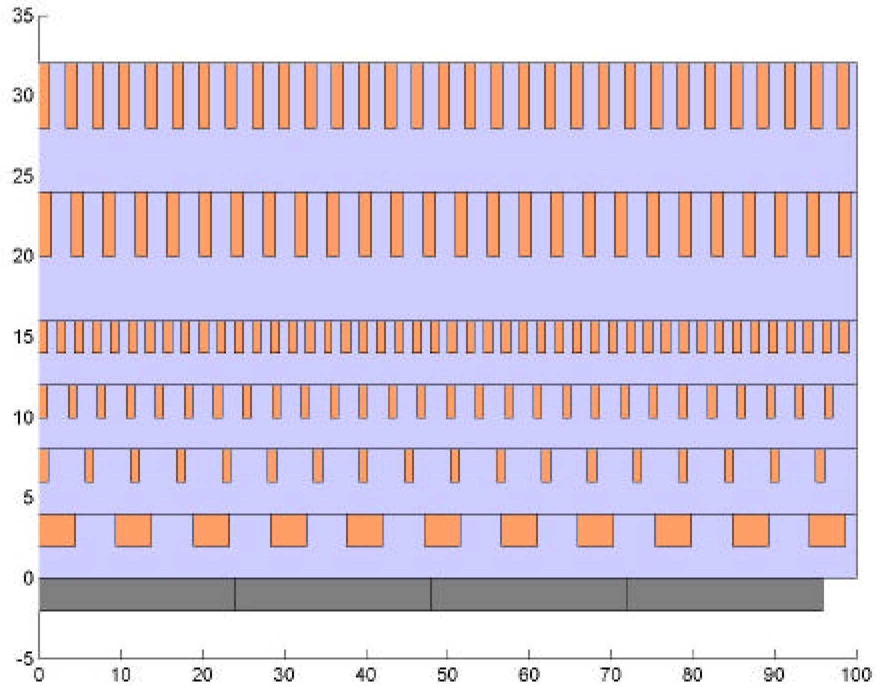
Results: GA Convergence

- Convergence of GA vs. number of samples
- Clock speed re-estimated using N_{samp} = 10,000

N_{samp}	Number of Generations	Normalized Speed of Convergence	Estimated Clock Speed (GHz)
1	76	1	1.1128
5	45	2.9605	1.0955
50	37	24.3421	1.1154
100	27	35.5263	1.1180

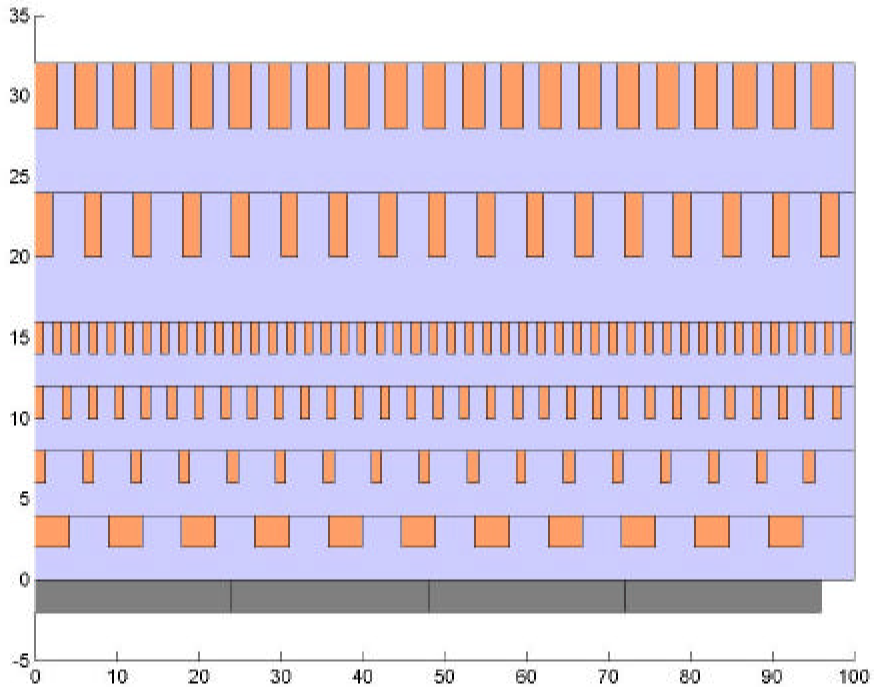
Results: Wiring Designs

- $N_{samp} = 50$
- Copper colored area represents wires
- Blue area represents dielectric
- Gray area represents silicon



Results: Wiring Designs

- $N_{samp} = 100$
- Copper colored area represents wires
- Blue area represents dielectric
- Gray area represents silicon



Conclusions

- GA was successfully used to design chip parameters using pre-layout analysis tools
- Because the GA re-evaluates the best designs, it is a good optimization scheme for stochastic objective functions
- GA shown to be relatively insensitive to value of N_{samp}
- Improved cycle time model can now be used in conjunction with Pareto optimization
  - Optimize a wiring layout for power dissipation, yield and clock speed