Optimized Pin Assignment for Lower Routing Congestion After Floorplanning Phase

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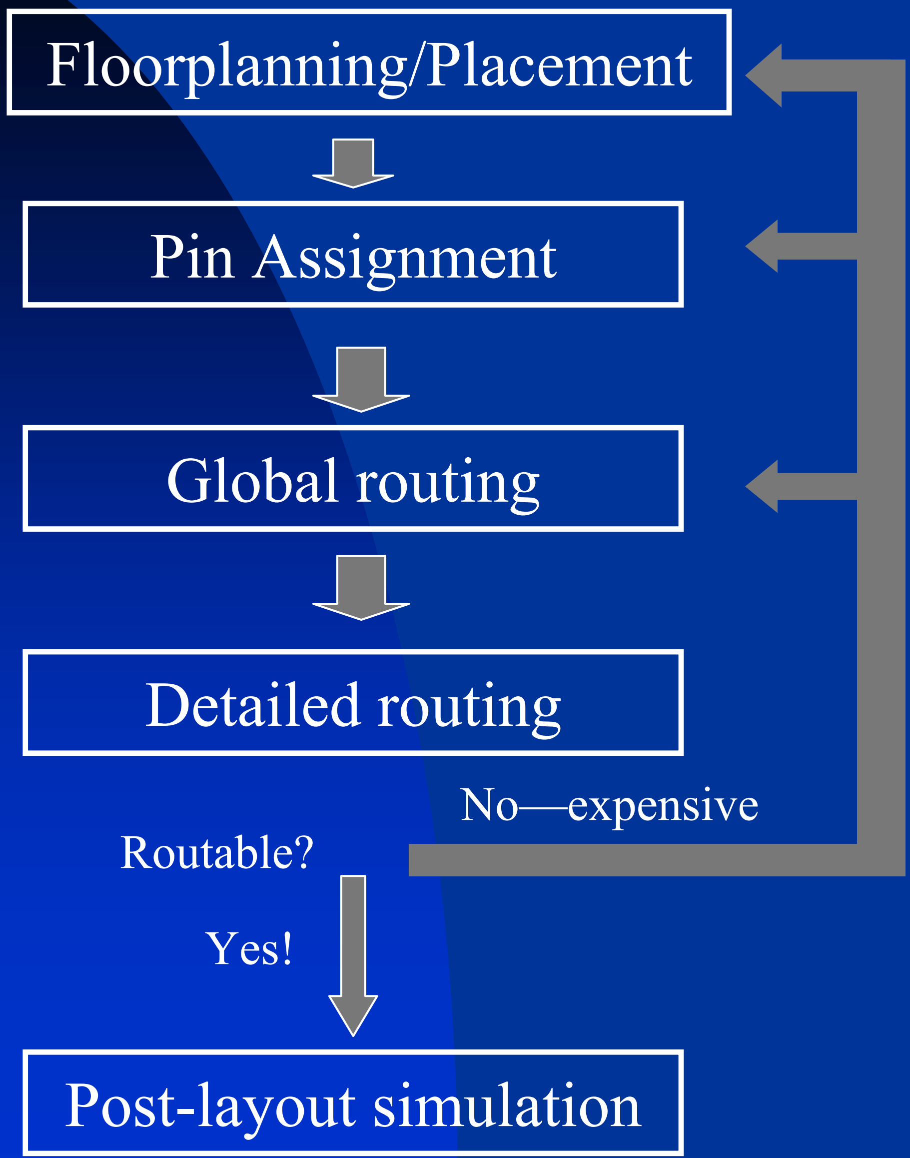
Introduction

- VLSI technology enters the age of Deep Submicron (DSM).
- Number of transistors approaches hundreds of million.
- More interconnects in circuit than ever results in a tight budget for “silicon real estate”.
- Successful routing of interconnects needs careful planning at the early phase of Physical Design.

Traditional Physical Design Flow

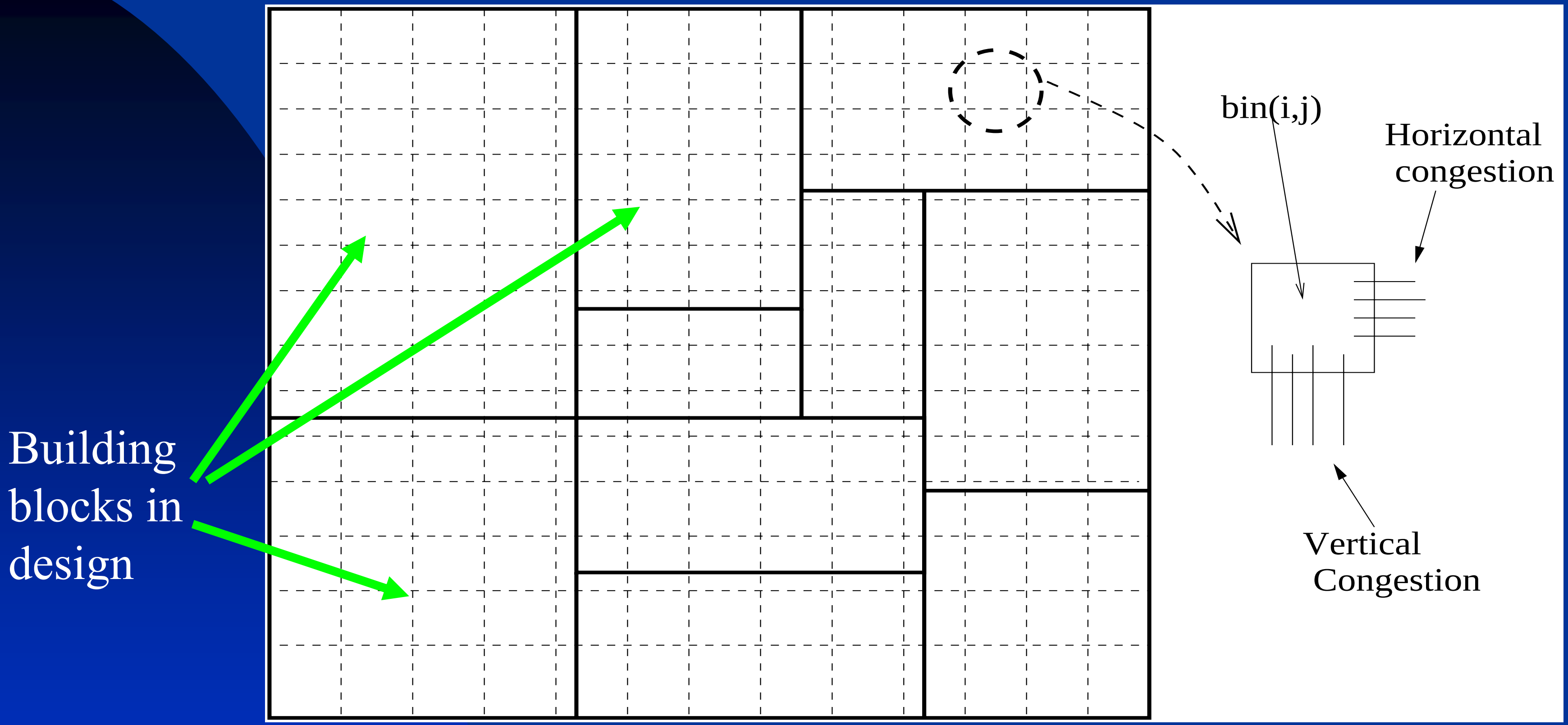


Our Strategy:

1) Estimate congestion information using statistical method after floorplanning phase.

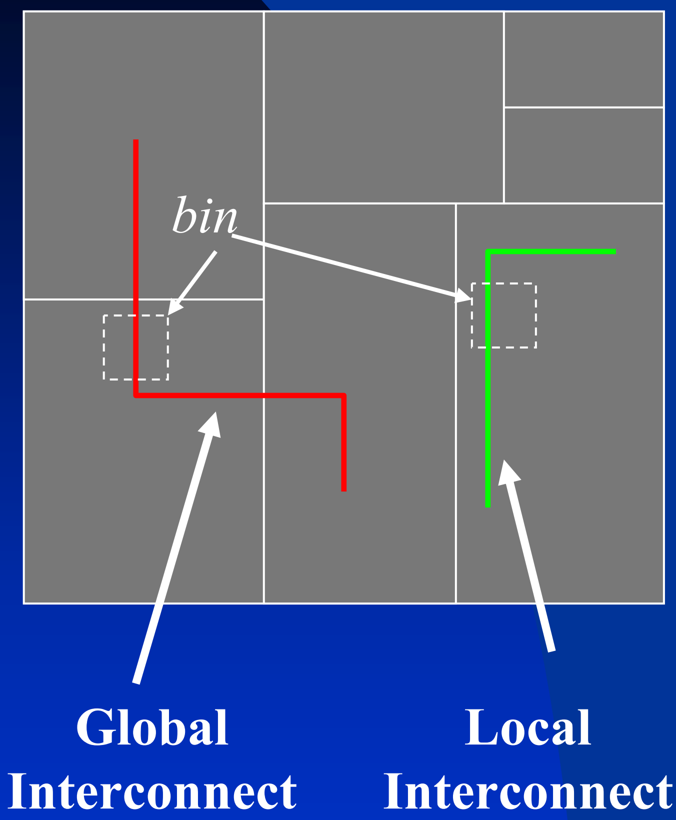
2) Based on congestion estimation, find optimized pin assignment to reduce routing congestion.

Global Bin and Congestion Metric



- If Congestion is larger than boundary capacity, overflow happens. $OV = C - Cap$
- Pin of global net belongs to a block. Pin assignment finds in which global bin of the block the pin should be located, so that routing congestion is minimized.

Congestion Classification



***Internal Congestion*: Congestion at bin boundary due to crossing of Local Interconnect.**

Estimation Strategy

No specific information about interconnect within blocks at floorplan phase.

Using Rent's Rule:

$$T = kN^{p}$$

***External Congestion*: Congestion at bin boundary due to crossing of Global Interconnect .**

Estimation Strategy

Statistical estimation based on Z-shape routing of global nets. Initial pin locations are also estimated statistically.

Internal Congestion Estimation

Rent's Rule: $T = kN^p$

N: number of gates in a logic subnetwork.

T: number of connections between this subnetwork and the rest of circuits.

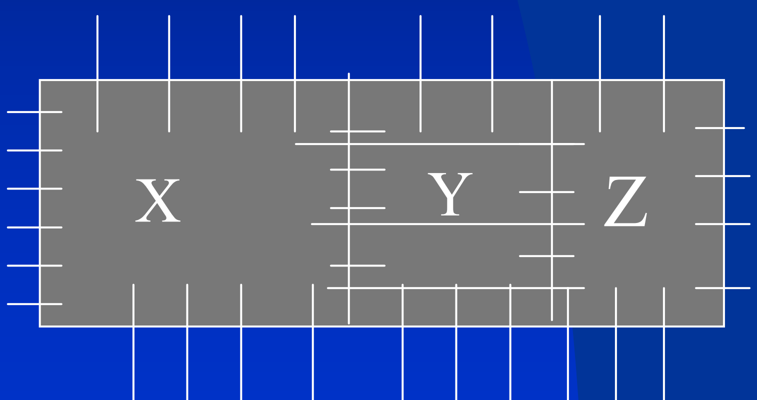
k: Rent's coefficient.

p: Rent's exponent.

\+ Conservation of I/O ports

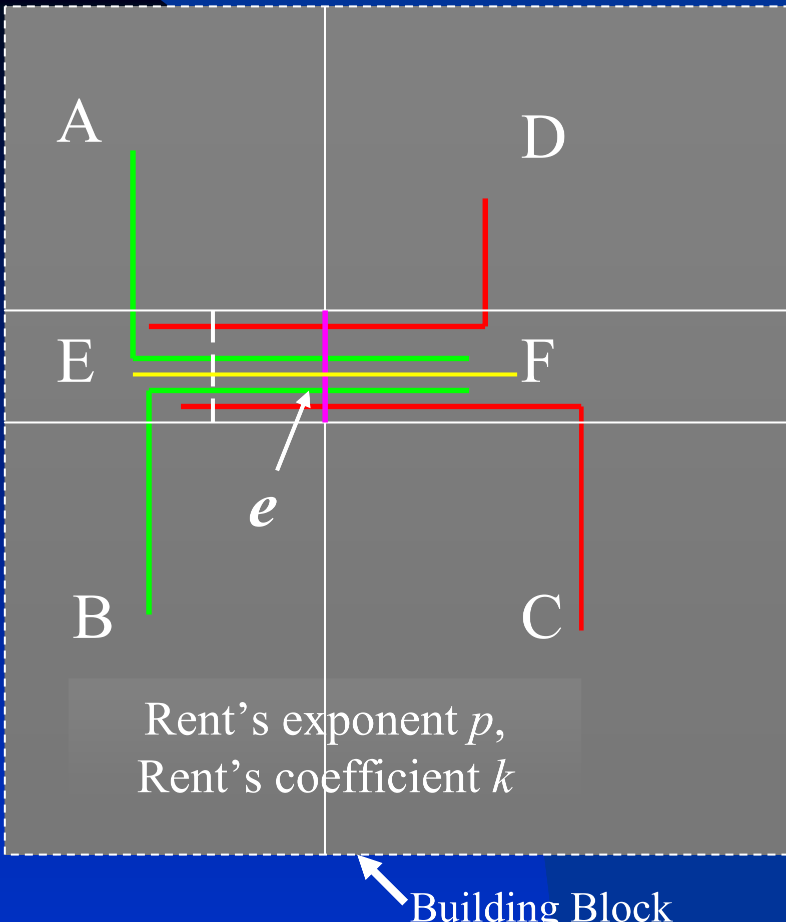
Estimation of the number of connections between two regions.

E.g.



$$T_{XtoZ} = k[(N_X + N_Y)^p + (N_Z + N_Y)^p - N_Y^p - (N_X + N_Y + N_Z)^p]$$

Internal Congestion Estimation



Edge *e* (of a global bin) decomposes building block into components A, B, C, D, E and F

Contribution to horizontal congestion at edge *e* includes: (Assume L-shape routing model)

- **Interconnection between components E and F.**
- **Interconnection between components A, B and F.**
- **Interconnection between components C, D and E.**

$$C_{h,e} = \frac{1}{1+\alpha}\left[T_{EtoF} + \frac{1}{2}\left(T_{ABtoF} + T_{CDtoE}\right)\right]$$

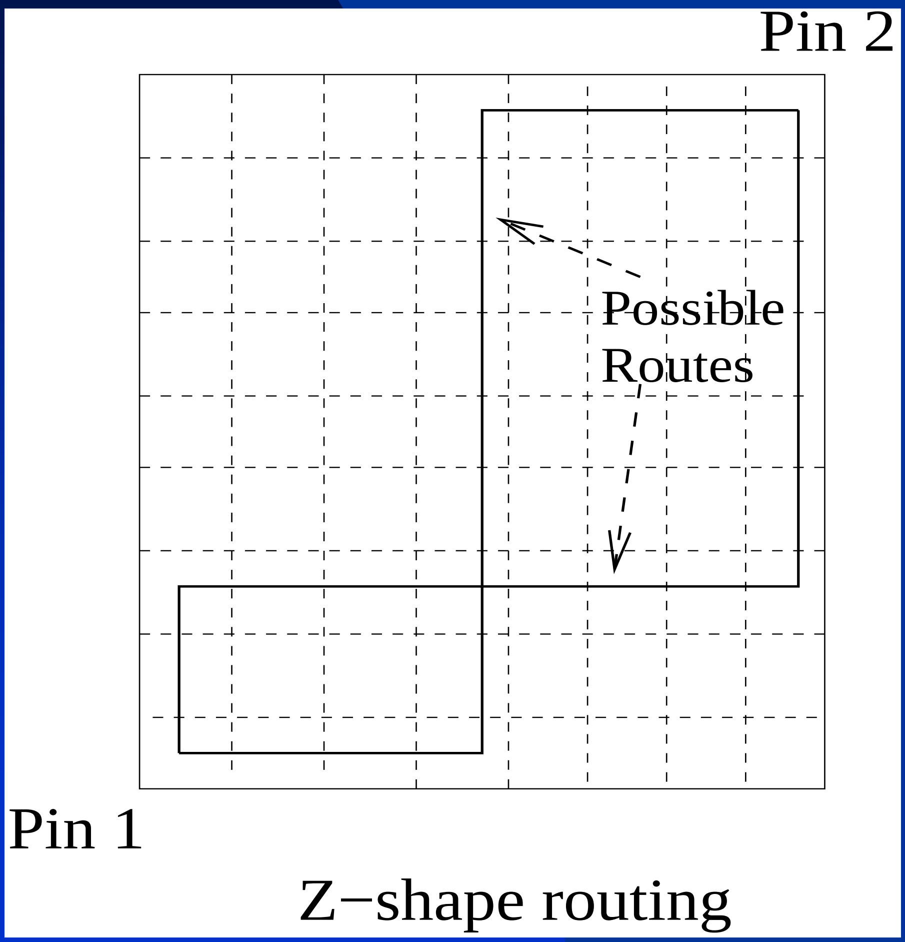
Horizontal congestion at *e*

α is average gate fan-out

There are two possible ways from AB to F and from CD to E

Global Routing and Pin Assignment Model

- **Best way to estimate external routing congestion is to apply a simple "real" routing, Z-shape routing.**



Number of possible routes R between two pins:

R = 1 when $x_1 = x_2$ or y1=y2

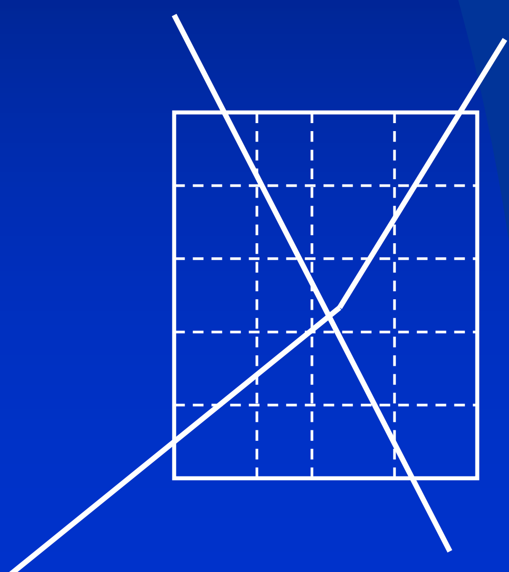
$R = |x_1 - x_2| + |y_1 - y_2|$ otherwise.

Global Routing and Pin Assignment Model

Simple Z-shape routing

Multiple-pin Net —PRIM MST / Edge cost: Manhattan distance→ **A set of two-pin nets**

Since routing is over-the-cell, pin can be anywhere in the block.

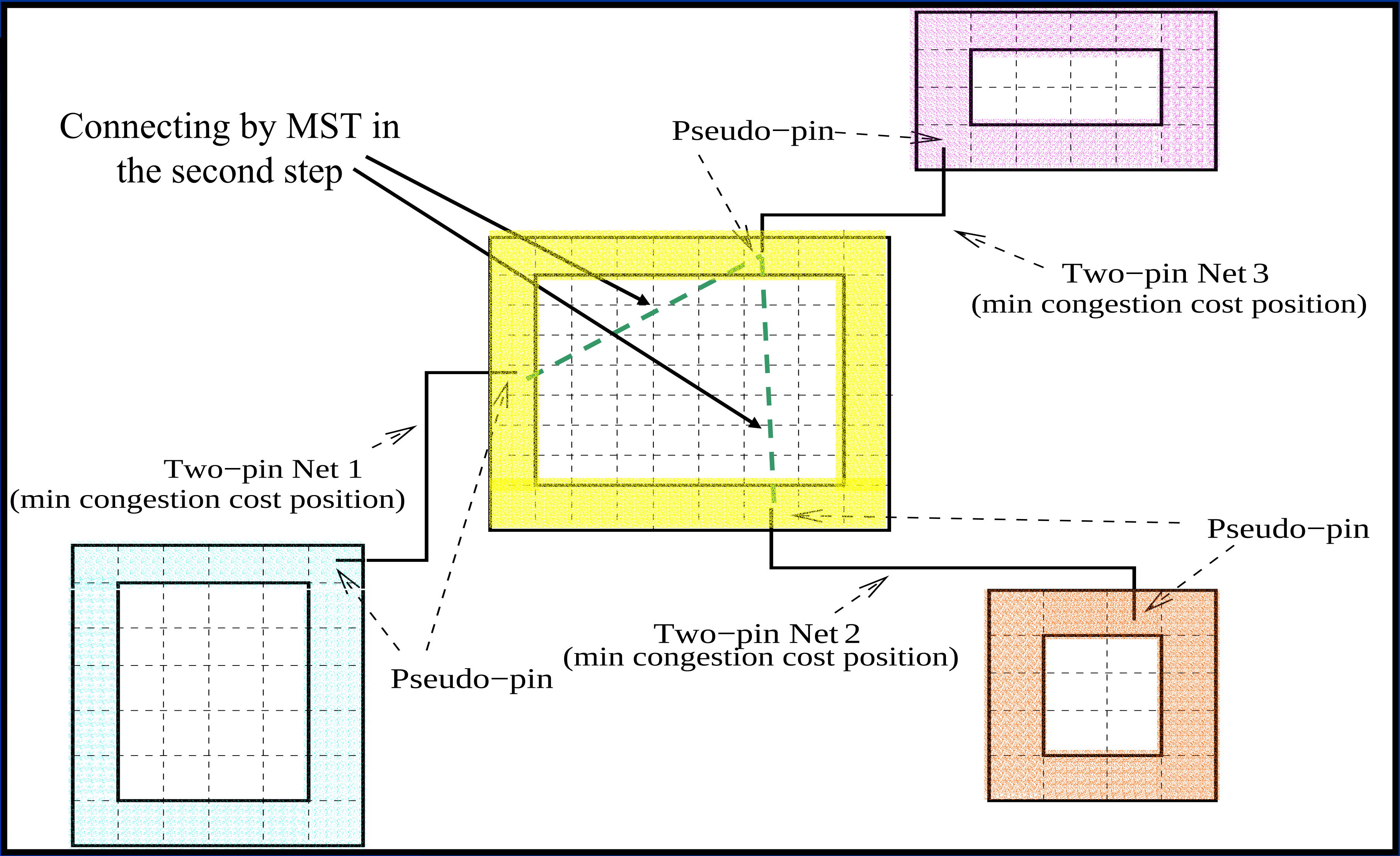


Problem: To find best pin locations of a net,

Computational complexity can be as high as

$O(n^d)$. n is number of bins in a block if assume they have same size, d is the degree of the net.

Global Routing and Pin Assignment Model



Decoupling of two-pin nets sharing the same pin. Block boundary are possible locations of "Pseudo-Pin"

Global Routing and Pin Assignment Model

Two-step strategy:

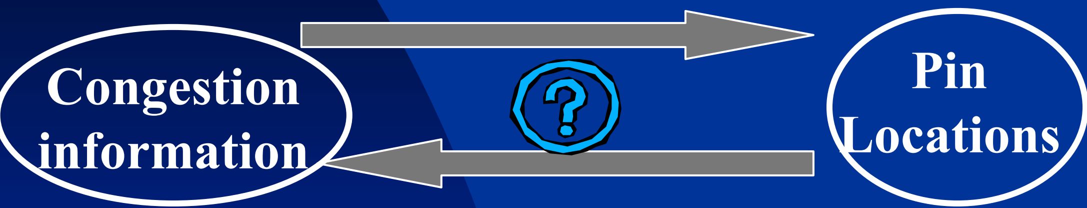
1. **Two-pin nets sharing the same pin are first decoupled. This shared pin is decomposed into pseudo-pins. Possible pseudo-pin locations are on the block boundary. Find best pseudo-pin locations for minimized routing congestion.**

2. **Apply another MST to optimally connect the best pseudo-pin locations to ensure electrical equivalence. Edge cost in MST is congestion cost function (described later).**

External Congestion Estimation

Chicken-Egg problem:

Based on congestion information, determine pin location



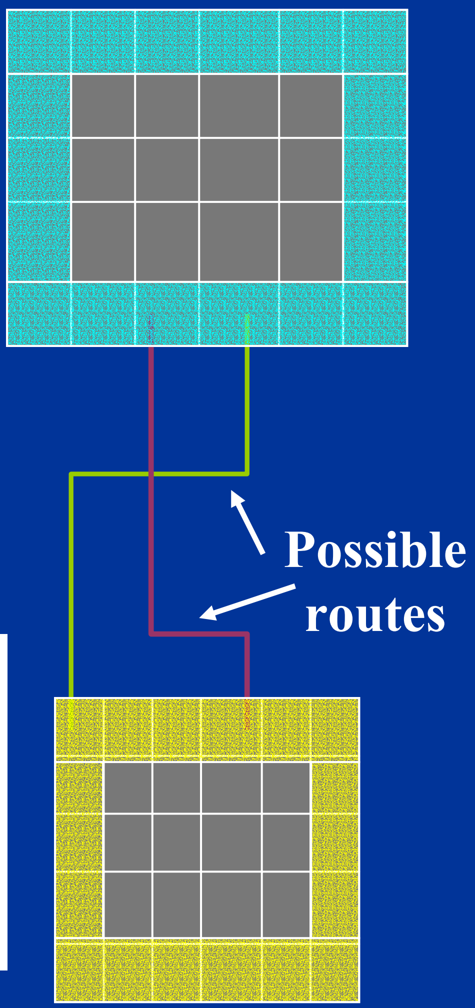
Based on pin location, do Z-shape routing, determine congestion information

To break dependence, apply an initial *probabilistic distribution* of pin locations.

Probability to take the route:

$$p_i = w_i \Big/ \sum_{all\ route\ j} w_j$$

$$w_i = \text{minCap} / L_i$$



minCap is minimum routing capacity along the route, L_i is the length of the route. Assign p_i to all the bin boundary along the possible routes.

Optimized Pin Location

- **Based on congestion graph (internal congestion and external congestion), least congested path is by minimizing the following path cost:**

$$Cost = \beta \sum_{\text{all bins}} OV^2 + \gamma \sum_{\text{all bins}} 1/diff^2 - \lambda Overlap^2$$

OV **is overflow at bin boundary --- punishment**

diff **is unused boundary capacity ---- preventive**

Overlap **is the overlap length with other route in same net ---- encouragement**

- **Find the lowest congestion cost path, so determine the optimized pin locations.**

Overall pin assignment algorithm

1. Based on Rent's Rule, estimate the internal congestion.
2. Decompose every multi-pin net into a group of two-pin nets using PRIM MST algorithm.
3. Estimate external congestion using Z-shaped routing model and probabilistic pseudo-pin location.
4. For each two-pin net, calculate congestion cost of all possible routes, find least cost route and determine the corresponding pseudo-pin location.
5. For all the pseudo-pins in the same block that correspond to the same pin, build an MST connecting them, and final pin location may correspond to the location of any pseudo-pin.

Experiment Results

Circuit	# of nets	# of blocks	grids	Horizontal overflow		Vertical overflow		run time (*sec*)
				OPA	RPA	OPA	RPA	
apte	97	9	20 x 20	95	134	44	88	145
ami33	123	33	30 x 30	280	432	191	443	184
ami49	408	49	30 x 30	306	413	27	215	176
xerox	203	10	20 x 20	0	160	1	149	93
hp	83	11	30 x 20	22	61	4	10	229

OPA: Optimized Pin Assignment

RPA: Random Pin Assignment

Conclusion

- After floorplanning phase, applying Rent's rule, circuit building block internal congestion is estimated.
- Based on an initial probabilistic pin location distribution, external congestion is estimated.
- With congestion map, an optimized pin assignment algorithm is proposed.
- Experiment results show effective reduction in routing congestion with optimized pin assignment.

Thank you!