Hierarchical Power Supply Noise Evaluation for Early Power Grid Design Prediction

M. Graziano, G. Masera, G. Piccinini, M. Zamboni

VLSI LAB. - Electronics Dep. - Politecnico di Torino
Outline

- Power Supply Noise
- Power Supply Noise Analysis
- Approaches
- Proposed methodology
- Results and conclusions
Power Supply Noise

\[ V_{\text{supply}} \Rightarrow V_{\text{ideal}} \]
Power Supply Noise

$V_{suppy} \Rightarrow V_{ideal}$

SSN $\Rightarrow L \cdot \frac{dI}{dt}$
Power Supply Noise

\[ V_{\text{supply}} \Rightarrow V_{\text{ideal}} \]

\[ \text{SSN} \Rightarrow L \cdot \frac{dI}{dt} \]

\[ \text{Voltage Drop} \Rightarrow R \cdot I \]
Power Supply Noise

\[ V_{\text{supply}} \implies V_{\text{ideal}} \]

\[ \text{SSN} \implies L \cdot \frac{dI}{dt} \]

\[ \text{Voltage Drop} \implies R \cdot I \]

\[ V_{\text{supply}} = V_{\text{ideal}} + L \frac{dI}{dt} + R \cdot I \]
Power Supply Noise

Resistance

- Metal line shrinking
- Skin effect
- Temperature
Power Supply Noise

- Resistance
  - Metal line shrinking
  - Skin effect
  - Temperature
  - Copper
  - Fat wires
Power Supply Noise

Inductance

Higher frequency

Complexity: return path
Power Supply Noise

Inductance

Higher frequency

Complexity: return path

Shielding

Flip Chip technology
Power Supply Noise

Current

Gate density increasing

⇒ higher currents

Higher frequency

⇒ \( \frac{dI}{dt} \) grows
Power Supply Noise

Capacitance

Fat wires

⇒ interconnect capacitance increases

Reduced gate sizes

⇒ reduced intrinsic decoupling

capacitance \Rightarrow \frac{dI}{dt} \text{ grows}
Power Supply Noise

Capacitance

Fat wires

⇒ interconnect capacitance increases

Reduced gate sizes

⇒ reduced intrinsic decoupling

capacitance ⇒ \( \frac{dI}{dt} \) grows

Low \( K \) materials
Power Supply Noise

Effects: direct

Gate delays, errors, failures
Power Supply Noise

**Effects: indirect**

- **Digital GND with SSN**
- **Voltage Transient**
- **Sensitive node**
- **Quiet analog GND**
- **Reverse biased junction capacitances**
- **Biased contact**

**Substrate injection**
Power Supply Noise

**Effects: indirect**

- VDD
- GND
- Data or clock signal
- Capacitance
- Parasitic coupling
- Injected signal
- Switching reference

**Crosstalk against signal lines**
Power Supply Noise

Effects: indirect

Board

Package

Chip

cable

Power Line

Direct

Emission

Signal Port Noise

Electro-magnetic Radiation

Power Line Conducting noise

Emi towards neighbours circuits

SLIP 2001 - M. Graziano
Power Supply Noise

Countermeasures

♦ Technologist: copper, Low-k, SOI, C4

♦ Circuit designer: decoupling capacitors, current limiters, logic family variation

♦ Physical designer: routing and placement strategies

⇒ early PSN evaluation
PSN evaluation

Power Supply Noise Evaluation Approaches

- Verification at the end of the design process: accurate but expensive
- Early analysis: has lower accuracy but gives a priori design parameters
Power Supply Noise Evaluation

- Power Grid Modeling
- Current Analysis

PSN Analysis
PSN evaluation

Power grid analysis approaches

- Hierarchical analysis
  - Extract parasitics of a macro power grid
  - Simplify it in a concentrated model for that macro
  - Use it for the higher hierarchical analysis
  - Can be extremely inaccurate: the distributed effect is lost
PSN evaluation

Current analysis approaches

- Vector producing worst switching activity
  - maximum switching \( \neq \) worst noise
- Simultaneous switching
  - too pessimistic upper bound
- Static timing analysis for current skew evaluation
  - too pessimistic: does not consider switching direction
PSN evaluation

Proposed method base on:

- **Hierarchical current activity algorithm:**
  - uses dynamic current informations (database)
  - consider switching direction
  - consider current skew
  - consider current in “no-switching” transitions

- **Hierarchical Power Grid model**
  - Infer distributed parasitic informations from lower to higher hierarchical levels
  - Include current informations for line sizing, parasitic evaluation and Power Supply Noise estimation
Proposed method

1. Define current activity (Current LUT, CAA, STA):
2. Define parasitics from line dimensions;
3. Compute power supply overvoltage (Model);
4. Define critical points;
5. Define possible solutions:
   5.1 Increasing critical points line width or/and
   5.2 Inserting decoupling capacitances or/and
   5.3 Equalizing current injection (placement, TDP)
Proposed method

Currents: library database

- Each library cell is simulated in all possible input transition state (implying or not output transition): current is measured
- Current activity types are clustered, coded and a sample is found
- A Look-up-table is generated for each input transition state from $V_{in} \rightarrow V_{out}$ and to $I_{in} \rightarrow I_{out}$
Proposed method

Currents: hierarchical analysis
Proposed method

Currents: hierarchical analysis

[Diagram of hierarchical analysis]
Proposed method

Currents: activity evaluation

![Diagram of a circuit with labeled nodes: I0, I2, I5, I4, I3, I7, I1, I6, and an output node labeled 'out'. The circuit includes gates and nodes labeled with variables 'a' and 'b'.]
Proposed method

Currents: activity evaluation

Diagram showing a circuit with nodes labeled I0 to I7 and inputs a and b.
Proposed method

Currents: activity evaluation

[Diagram of a circuit with labeled currents I0 to I7 and inputs a and b]
Proposed method

Currents: activity evaluation

[Diagram showing a circuit with labeled currents and inputs]
Proposed method

Currents: activity evaluation

SLIP 2001 - M. Graziano
Proposed method

Currents: activity evaluation

SLIP 2001 - M. Graziano
Proposed method

Currents: activity evaluation

\[ \begin{align*}
I_0 & \rightarrow T_0 \\
I_2 & \rightarrow T_2 \\
I_5 & \rightarrow T_5 \\
I_4 & \rightarrow T_4 \\
I_1 & \rightarrow T_1 \\
I_3 & \rightarrow T_3 \\
I_6 & \rightarrow T_6 \\
I_7 & \rightarrow T_7 \\
\end{align*} \]
Proposed method

Currents: activity evaluation

\[ I_0 \text{ current skew} \]
\[ I_2 \text{ current skew} \]
\[ I_5 \text{ current skew} \]
\[ I_4 \text{ current skew} \]
\[ I_1 \text{ current skew} \]
\[ I_3 \text{ current skew} \]
\[ I_6 \text{ current skew} \]
\[ I_7 \text{ current skew} \]

SLIP 2001 - M. Graziano
Proposed method

Power grid: ROW

Row $r$, $N$ gates
Proposed method

Power grid: MACRO

Macro m, K rows
Proposed method

Power grid: BLOCK

Block b, M macros
Proposed method

Power grid: ROW

\[ V_{rN} = V_{r0} + N R_r I_{rIN} + N L_r \frac{d}{dt} I_{rIN} + R_r \sum_{i=1}^{N} \left( i (I_{gi} - I_{ci}) \right) \]

\[ + L_r \sum_{i=1}^{N} \left( i \frac{d}{dt} (I_{gi} - I_{ci}) \right) \]
Proposed method

Power grid: MACRO

\[ V_{kK} = V_{k0} + K R_k I_{kIN} \]
\[ + K L_k \frac{d}{dt} I_{kIN} + R_k \sum_{i=1}^{K} \left( i(I_{gi} - I_{ci}) \right) \]
\[ + L_k \sum_{i=1}^{K} \left( i \frac{d}{dt} (I_{gi} - I_{ci}) \right) \]
Proposed method

Power grid: BLOCK

\[ V_{mM} = V_{m0} + M R_m I_{mIN} \]

\[ + M L_m \frac{d}{dt} I_{mIN} + R_m \sum_{i=1}^{M} \left( i (I_{gi} - I_{ci}) \right) \]

\[ + L_m \sum_{i=1}^{M} \left( i \frac{d}{dt} (I_{gi} - I_{ci}) \right) \]
Methodology results and conclusions

- Results for non automated evaluations on a two macros block with 25 gates each showed with respect to HSPICE simulations:
  - Accuracy in current waveform evaluation of 98%
  - Accuracy in worst power supply noise evaluation of 85% due to parasitic modeling
- Needs final implementation for managing complex circuits and benchmarks
- Need further improvements in parasitic modeling
- Expected good results in terms of accuracy and efficiency