Power Supply Design
Parameters Prediction for High Performance IC Design Flow

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Summary

- Introduction: noise in VLSI circuits
- IR drop and $L \frac{dI}{dt}$ causes, scale and consequences
- Proposed methodology to face these problems
- Power Supply Model
- Noise cost function
- Conclusions
Introduction: noise in VLSI circuits

Technology scaling down leads to:

- increasing chip size
- increasing clock frequency
- increasing interconnect density

\[ \Rightarrow \text{noise jeopardizes } UDSM \text{ circuits functionality:} \]

- crosstalk
- electromigration
- ground bounce
- IR drop

\[ L \frac{dI}{dt} \]
IR drop and $L\frac{dl}{dt}$.

IR drop causes

Transistor and interconnection scaling down causes

- increased gate number w/o area change
  - greater number of gates in a row
  - growing current on power supply lines
- increased line resistance
  \[\downarrow\]
- increased $GND$ and $VDD$ area for electromigration
- rise of **IR drop**
IR drop and \( L \frac{dI}{dt} \) causes

Transistor sizes scaling down causes:

- Increased frequency of the clock signal
- Higher gate switching activity
- Higher electromigration risk
- Decreased clock rise time: higher \( L \frac{dI}{dt} \) for on-chip and package inductances
IR drop and $L \frac{dI}{dt}$ influences on Power Supply

- Higher sensibility of gates to noise spikes: delay, charge alteration, reduced $V_t$
- Crosstalk towards neighbor lines
- EMI problems towards neighbor circuits
- Ground bounce injected into the substrate
IR drop and L dl/dt simulations

IR drop influence: simulations

IR drop: simulation parameters

- AND2 TSPC, 0.25μm, 2.5V, 1Ghz
- Growing number of cells: from 200 up to 600
- Different parasitic inductance conditions: on chip distributed (0.2pH), package (1pH – 10pH)
- Distributed parasitic resistance function of electromigration sizing
IR drop and $L \frac{dl}{dt}$ Simulations

IR drop: simulations results

- 0.2pH, Dist.
- 1pH, Pack.
- 10pH, Pack

Noise Overshoot [V]

- 200 gates
- 400 gates
- 600 gates

Noise Width [ps]

**Methodology.**

**Verification or prediction?**

- Verification of noise failures has expensive time-to-market aftereffects.
- Countermeasures are strongly joined to designer intervention.
- It’s basic to develop design tools facing early in the design sequence the potential noise generation.

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Methodology.

Noise Cell Views and Cost Function

- Layout
- HDL
- Netlist
- Noise Injection Cell View
- Noise Tolerance Cell View
- Area
- Interconnect Density
- Delay
- Power
- NOISE COST FUNCTION

FLOORPLANNING AND PLACEMENT ALGORITHMS

Methodology: instruments

Synergy among tools related to different design phases is needed:

- transistor sizing optimization tool
- gate noise tolerance analysis
- cell model with noisy power supply references
- row of cells model: the influences between the cell and its environment

The maximum current is

$$I_{s1} = I_{sN+1} + N \cdot I_p$$

while the worst overvoltage is

$$V_N = V_0 + N \left( R I_{sN+1} + L \frac{d}{dt} I_{sN+1} \right) + \frac{N(N+1)}{2} \left( R I_p + L \frac{d}{dt} I_p \right)$$
Maximum noise overvoltage is known from the number of cells inserted on the line, or vice-versa.

As a drawback the area of a GND line is:

\[ A_{\text{line}} = N \cdot l_{\text{gate}} \cdot w_{\text{MAX}} \]
Area optimization without noise worsening

- Area waste due to \textit{worst current} value used to dimension the whole line

- \textbf{Ideal sizing:} \textit{GND} and \textit{VDD} line width for cell \textit{i} proportional to the maximum current at point \textit{i}

- \textbf{Real sizing:} a controlled and optimized line segmentation is proposed

Optimized dimensioning

\[ g(M - 1) = M - 1 \]

\[ \Delta w = \frac{w_{\text{max}} - w_{\text{min}}}{g(M - 1)} \]

Optimized dimensioning: gain and loss

The area gain is

$$\Delta_A = -\frac{l_N}{2} \left( w_{MAX} - w_{MIN} \right)$$

and the noise loss due to increased resistance is:

$$\frac{\Delta_N}{T} = \left( \frac{I_{s,N+1}}{I_{s1}} \left( \frac{1}{M} \sum_{m=1}^{M} f_m - 1 \right) + \frac{I_p}{I_{s1}} \cdot \left( \frac{1}{2} \frac{1}{M} \left( \frac{N}{M} + 1 \right) \right) \cdot \sum_{m=1}^{M} f_m + \frac{N}{M^2} \sum_{m=1}^{M} (M - m) f_m - \frac{N + 1}{2} \right)$$

where

$$R_m = \frac{R}{N} \frac{l_N}{w_{MAX}} \frac{1}{f_m(m, w_{MIN}, g(m - 1))}$$
Optimized dimensioning: overvoltage control

Losses at node N when optimizing for area: N parametric

\[ \Delta N \]

\[ T \]

\[ \Delta A \]

2 cells for block m
20 cells for block m
100 cells for block m
area gain

\[ w_{\text{min}} = \text{TEC}_{\text{MIN}} \]
\[ W_{\text{MIN}} \]
\[ w_{\text{min}} = w_{\text{MAX}} \]
Using a good number of segments with increasing dimensions the number of cells does not influence the loss in noise safety.

The designer has control on area and noise, varying:

- number of gates in a row \( N \)
- number of segments having different width \( M \)
- width at the line endpoints \( w_{\text{MAX}}, w_{\text{MIN}} \)
Noise reduction: distributed capacitors

Maximum overvoltage versus distributed capacitors

- 200 gates
- 400 gates
- 600 gates

Overshoot [V] vs. Distributed capacitance [fF]
Power Supply Model. Noise reduction

**Decreased current to shrink resistance**

- **a)**
  \[ Is_i = I_p + Is_i+1 \]

- **b)**
  \[ Is_i = (I_p - I_c) + Is_i+1 \]

- **c)**

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Distributed capacitors: loss and gain

Noise overshoot variation

\[ V_N \bigg|_{\text{cap}}^{w_{\text{MAX}}} - V_N = R \cdot t \cdot \frac{N}{2} - R \cdot t \cdot \frac{N}{2} \cdot \frac{I_c}{I_p} \left( l_{\text{gate}} + l_{\text{cap}} \right) \]

Area variation

\[ A_{\text{line}} \bigg|_{\text{cap}}^{w_{\text{MIN}}} - A_{\text{line}} = \frac{l_{\text{cap}}}{t} \cdot N^2 \cdot I_p - \frac{l_{\text{gate}} + l_{\text{cap}}}{t} \cdot N^2 \left( I_p - I_c \right) \]
Distributed capacitors design parameters

If the line width is chosen between

\[ N \left( \Pi_p - \Pi_c \right) \left( 1 + \frac{l_{gate}}{l_{cap}} \right) < w < \frac{N \Pi_p}{t} \frac{l_{gate}}{l_{gate} + l_{cap}} \]

and each cell in the library is connected to an optimized capacitor, a gain in noise and in area is assured with respect to the case w/o capacitors.
Future model developments

- conjunction of optimized dimensioning and of distributed capacitors insertions
- $I_p = I_p(t)$ and $V_N = V_N(t)$
- clock skew modeling in the current superposition and overvoltage evaluation
- package influence on row model
- extension to S.O.C. designs
A Noise Cost Function to be introduced in a placement algorithm is influenced as shown before by

- Noise overvoltage
- Power supply lines area
- Electromigration
- Number of cells in a row
- Distributed optimized capacitors
- Number of optimized segments
Conclusions

♦ The aim is to create a NOISE COST FUNCTION to be inserted in a placement algorithm

♦ it is based on:
  ♦ a cell description with noise characteristics
  ♦ a cell environment description with noise generation parameters

♦ it is of basic impact to face early in the design sequence the potential noise aftereffects