27th ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP)

www.SLIPonline.org

Co-located with ACM/IEEE Intl. Conf. on Computer-Aided Design Conference in Munich, Germany on October 30, 2025

GENERAL INFORMATION

2025 SLIP is the 27th edition of the Workshop. SLIP will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect that span system, application, design, and technology.

The technical goal of the workshop is to identify fundamental problems, and foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, STCO/DTCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, backside metallization, and new fabrics for the beyond-Moore era.

Organizing & Steering Committee:

Mustafa Badaroglu (Qualcomm)
Seungwon Kim (Cadence)
Dirk Stroobandt (Ugent)
Baris Taskin (Drexel Univ)

TECHNICAL TOPICS

- Technical topics include but are not limited to:
- Learning and predictive models for interconnect at various IC and system design stages
- Pathfinding of on-chip interconnect, backside metallization, 2.5D/3D chip-to-chip communication interfaces, and optical IOs/links
- System-level design for FPGAs, NoCs, AI/compute accelerator for scale-up and scale-out scalability
- Design, analysis, and (co)optimization of power, clock distribution networks, and memory pools
- Compute near/in-memory processing for LLM workloads
- System-level interconnect reliability, aging, thermal, yield and cost issues
- Predictive models for power and performance of system-level interconnects

IMPORTANT DATES

Abstract Registration:	September 1, 2025
Author Notification:	September 8, 2025
Presentation Upload:	September 22, 2025
Workshop:	October 30, 2025