24th ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP)

www.SLIPonline.org

Co-located with ACM/IEEE Intl. Conf. on Computer-Aided Design Conference

November 3, 2022

Hybrid: In-Person or Virtual Workshop

Co-sponsored by ACM SIGDA and IEEE Computer Society TCVLSI

Accepted papers are published in an IEEE/ACM proceedings

GENERAL INFORMATION

The 2022 ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP) is the 24th edition of the Workshop.

SLIP, co-located with ICCAD 2022, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology.

The technical goal of the workshop is to identify fundamental problems, and foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, DTCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, and new fabrics for the beyond-Moore era.

The submission process consists of two steps: abstract registration followed by regular technical paper submission in 4 to 6 pages plus 1 page of references, double-column, 9pt/10pt font in ACM proceedings format. To permit blind review, all papers must remove author information. Authors should submit papers electronically: https://easychair.org/conferences/?conf=slip2021

One author of accepted submission will present the work at the workshop. Accepted technical papers will be published in the ACM and IEEE digital libraries.

TECHNICAL TOPICS

Technical topics include but are not limited to:

- Learning and predictive models for interconnect at various IC and system design stages
- Roadmapping and pathfinding of on-chip interconnect and 2.5D/3D chip-to-chip communication interfaces
- System-level design for FPGAs, NoCs reconfigurable systems, and domain-specific multi/many-core systems
- Design, analysis, and (co)optimization of power, clock distribution networks, and memory partitioning systems
- System-level interconnect reliability, aging, thermal, yield and cost issues
- Predictive models for power and performance of system-level interconnects
- Interconnects in bio-inspired systems, such as artificial neural networks and quantum architectures

SPECIAL SESSIONS

- Power distribution in advanced technology nodes
- Tackling memory wall in many-core and AI systems

IMPORTANT DATES

Abstract Registration: August 8, 2022
Paper Submission: August 15, 2022
Author Notification: September 2, 2022
Final Version Upload: September 11, 2022

General Chair: Mustafa Badaroglu (Qualcomm)
Steering Committee: Andrew Kahng (UC San Diego), Dirk Stroobandt (UGent), Baris Taskin (Drexel Univ)
Technical Program Chair: Shantanu Dutt (Univ. Illinois at Chicago)
Keynotes and Special Sessions Chair: Pascal Vivet (CEA)
Publicity Chair: Ismail Bustany (AMD)
Publication Chairs: Rasit Topaloglu (IBM), Seungwong Kim (UCSD)