The technical goal of the workshop is to (1) identify fundamental problems, and (2) foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, DTCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, and new fabrics for the beyond-Moore era. Technical topics include but are not limited to:

- Learning and predictive models for interconnect at various IC and system design stages
- Roadmapping and pathfinding of on-chip interconnect and 2.5D/3D chip-to-chip communication interfaces
- System-level design for FPGAs, NoCs, reconfigurable systems, and domain-specific multi/many-core systems
- Design, analysis, and (co)optimization of power, clock distribution networks, and memory partitioning systems
- System-level interconnect reliability, aging, thermal, yield and cost issues
- Predictive models for power and performance of system-level interconnects
- Interconnects in bio-inspired systems, such as artificial neural networks and quantum architectures

There are two special sessions this year:
1. 3DIC architectures and high-speed energy-efficient on/off-chip interconnects
2. DTCO-enhanced physical design and EDA flows

**Format:**
More interactive, workshop-like tone and format despite being held virtually this year. The workshop includes keynotes, regular paper sessions, and invited talks.

**Keynote Talks:**
1. Always-on edge-AI and connectivity, Dr. Evgeni Gousev (Qualcomm)
2. 3DIC architectures and chiplets for heterogeneous computing, Dr. Tanay Karnik (Intel)

**Submission:**
We invite authors to submit papers of 4 to 8 pages, double-columned, 9pt/10pt font in ACM proceedings format available at: [https://www.acm.org/publications/proceedings-template](https://www.acm.org/publications/proceedings-template).

To permit double blind review, all papers must remove author information. Authors should submit papers electronically via: [https://easychair.org/conferences/?conf=slip2021](https://easychair.org/conferences/?conf=slip2021)

Accepted papers are published in IEEE/ACM proceedings and listed by IEEE Xplore.

**Important Dates:**
- Abstract Registration: August 8, 2021
- Paper Submission: August 15, 2021
- Author Notification: August 31, 2021
- Final Version Upload: September 10, 2021

**Technical Program Committee:**
- **Co-Chairs:** Brian Cline (Arm), Ismail Bustany (Xilinx)
- **Members:** Ivan Ciofi (imec), Titashe Rakshit (Qualcomm), Shantanu Dutt (Univ. Illinois at Chicago), Rasit Topaloglu (IBM), Payman Zarkesh-ha (Univ New Mexico)
- **Special Sessions Co-Chairs:** Pascal Vivet (CEA), Yuzo Fukuzaki (TechInsights)

---

23^rd^ ACM/IEEE International Workshop on System-level Interconnect Pathfinding (SLIP)

Co-hosted with ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD)

**November 4, 2021**
**Virtual Event**

Co-sponsored by ACM SIGDA and IEEE Computer Society TCVLSI

[www.sliponline.org](http://www.sliponline.org)

Accepted papers are published in IEEE/ACM proceedings.